BUDDHA SERIES

(Unit Wise Solved Question & Answers)

Course – B. Tech

College – Buddha Institute of Technology

(AKTU CODE-525)

Department: Applied Science and Humanities

Subject: Fundamental of Electronics Engineering

(BEC-101)

Faculty Name: Rahul Jaiswal & Sandeep Singh

BEC101 / BEC201 : FUNDAMENTALS OF ELECTRONICS ENGINEERING

Topics	Contact Hours
Unit-1	**8**
Semiconductor Diode: Depletion layer, V-I characteristics, ideal and practical Diodes, Diode Equivalent Circuits, Zener Diodes breakdown mechanism (Zener and avalanche) **Diode Application:** Diode Configuration, Half and Full Wave rectification, Clippers, Clampers, Zener diode as shunt regulator, Voltage-Multiplier Circuits **Special Purpose two terminal Devices:** Light-Emitting Diodes, Photo Diodes, Varactor Diodes, Tunnel Diodes.	
Unit-2	8
Bipolar Junction Transistor: Transistor Construction, Operation, Amplification action. Common Base, Common Emitter, Common Collector Configuration **Field Effect Transistor:** Construction and Characteristic of JFETs. Transfer Characteristic. MOSFET (MOS) (Depletion and Enhancement) Type, Transfer Characteristic.	
Unit-3	8
Operational Amplifiers: Introduction, Op-Amp basic, Practical Op-Amp Circuits (Inverting Amplifier, Non-inverting Amplifier, Unit Follower, Summing Amplifier, Integrator, Differentiator).Differential and Common-Mode Operation, Comparators.	
Unit-4	8
Digital Electronics: Number system & representation, Binary arithmetic, Introduction of Basic and Universal Gates, using Boolean algebra simplification of Boolean function. K Map Minimization upto 6 Variables.	
Unit-5	8
Fundamentals of Communication Engineering: Basics of signal representation and analysis, Electromagnetic spectrum Elements of a Communication System, Need of modulation and typical applications, Fundamentals of amplitude modulation and demodulation techniques. **Introduction to Wireless Communication:** Overview of wireless communication, cellular communication, different generations and standards in cellular communication systems, Fundamentals of Satellite & Radar Communication.	

UNIT-1

Ques 1 : What do you mean by Varactor diode? Write its one application. (AKTU : 2022-23)

(2 marks)

Sol. **Varactor diode** is the one which works on the principle of variation in capacitance by changing the width of the depletion region of P-N junction. The P-N Junction diode creates **capacitor effect**. The capacitance is controlled by applied voltage. It works on **reverse biased** mode. Varactor word is formed from words **Variable reactance** or **variable resistor**. Thus, it provides variable resistance or reactance or capacitance thus it is named as a varactor diode. The symbol of the varactor diode is same as conventional diode except the symbol of the capacitor is merged with the symbol of the diode to show the capacitance effect.

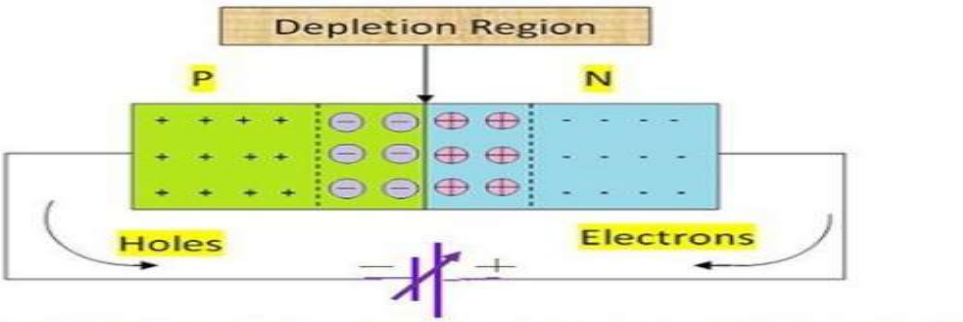
Symbol

Working of Varactor Diode

When the reverse bias is applied to P-N junction, the width of depletion layer increases. And with the increase of reverse voltage gradually the depletion layer increases even more. Thus, the depletion region creates Transition capacitance $C_{T.}$

$$C_T = \varepsilon A/W$$

Here, C_T is Transition capacitance, ε is dielectric constant, A is the area of plates of the capacitor and W is the width of the depletion layer.



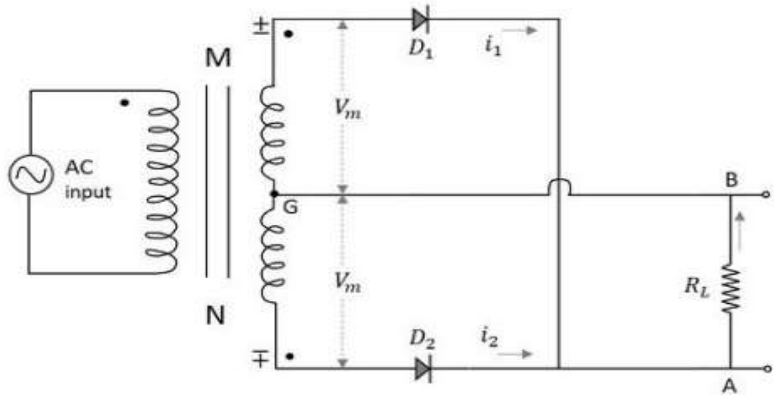
Depletion Region in a Reverse Biased P-N

Applications of Varactor Diode

1. **Television receivers:** Varactor diodes are used as tuned capacitors and have replaced mechanically tuned capacitors in various applications. It is used in television in the resonant tank circuit.
2. **Radio receivers:** Radio receivers also use this diode for tuning purposes.
3. **Frequency Multiplier:** It is also used as a frequency multiplier in various electronic circuits.
4. **Phase Locked Loops:** It is used in Phase locked loop for frequency modulation. Varactor diodes help in achieving frequency modulation. Thus, in communication devices varactor diodes are significant.
5. **Voltage controlled oscillators:** Voltage control oscillators are used extensively in transmission and receiving circuits in communication. And varactor diode plays a significant role in construction of voltage controlled oscillator.

Ques 2 : Draw and Explain the working of Centre-taped full wave rectifier . Also calculate its efficiency and ripple factor. (AKTU : 2022-23) (7 marks)

Sol. Center Tap Full Wave Rectifier: A Center Tap FWR circuit consists of 3 main parts: A transformer, A resistive load and Two diodes A Center Tap FWR circuit diagram looks like this:



Working Analysis:

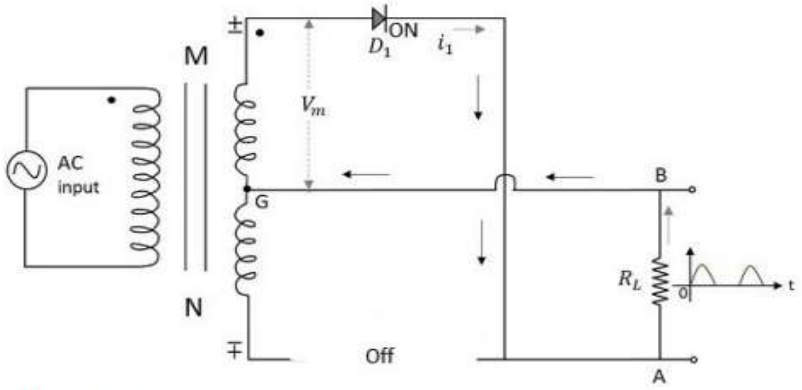
When $V_i > V_K$, D_1 is ON, D_2 is OFF

Drop across D_1 is V_K .

Applying KVL,

$V_i - V_K - V_0 = 0$

Or, $V_0 = V_i - V_K$ ---------- (i)



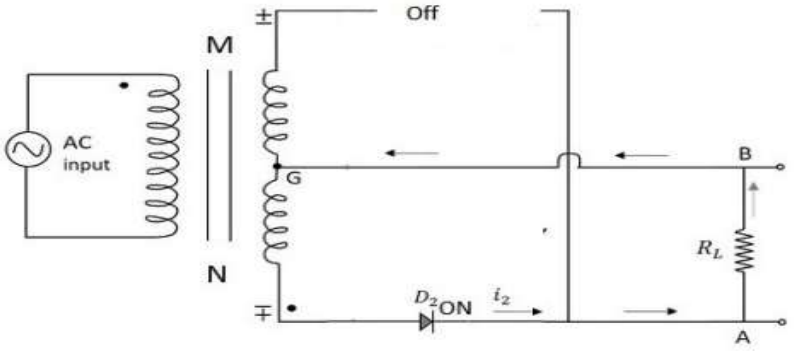
When $V_i < -V_K$, D_1 is Off, D_2 is ON

Drop across D_2 is V_K .

Applying KVL,

$$-V_i - V_K - V_0 = 0$$

Or, $V_0 = -V_i - V_K$ ---------- (ii)

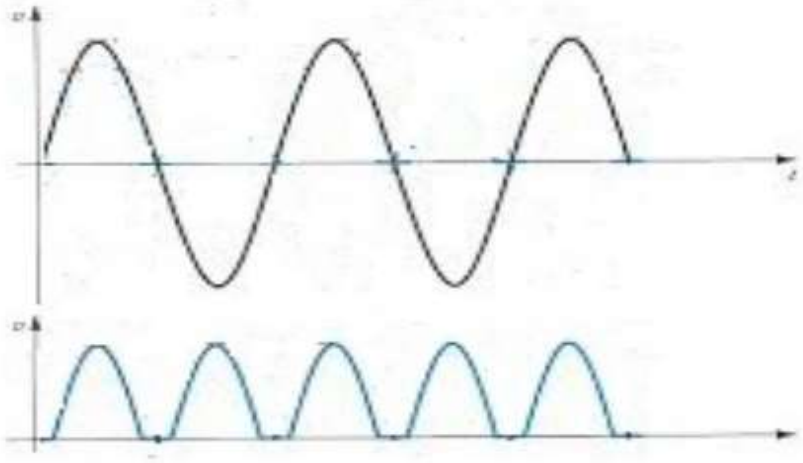


A

Diodes: Output Waveform:

Case 1: when $V_i > V_K$, $V_0 = V_i - V_K$

Case 2: when $V_i < -V_K$, $V_0 = -V_i - V_K$



Calculation of Efficiency: Efficiency of a rectifier is defined as the ratio of output DC power to input RMS power. It is denoted by η.

$$Then, \eta = \frac{P_{dc}}{P_i} = \frac{P_{dc}}{P_{rms}}, \quad where\ P_{dc} = I_{dc}^2 R_L\ and\ P_{rms} = I_{rms}^2 \left(R_L + R_f\right)$$

$$So, \quad \eta = \frac{P_{dc}}{P_{rms}} = \frac{I_{dc}^2 R_L}{I_{rms}^2 \left(R_L + R_f\right)} \quad But, R_f << R_L\ hence\ neglecting\ R_f$$

$$\eta = \frac{P_{dc}}{P_{rms}} = \frac{I_{dc}^2}{I_{rms}^2} = \left(\frac{I_{dc}}{I_{rms}}\right)^2$$

$$I_{avg} = I_{dc} = \frac{2I_m}{\pi} \quad and \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\eta = \left(\frac{I_{dc}}{I_{rms}}\right)^2 = \left(\frac{2I_m/\pi}{I_m/\sqrt{2}}\right)^2 = \frac{8}{\pi^2} \times 100 \quad \% = 81 \quad \%$$

Calculation of Ripple Factor (r): Ripple is defined as unwanted ac component present in the DC output of rectifier circuit. Ripple factor is defined as the ratio of ac component to DC output.

We know that

$$I_{rms}^2 = I_{ac}^2 + I_{dc}^2 \quad or, \quad I_{ac}^2 = I_{rms}^2 - I_{dc}^2, \quad devide\ equation\ by\ I_{dc}^2$$

$$\frac{I_{ac}^2}{I_{dc}^2} = \frac{I_{rms}^2}{I_{dc}^2} - 1 \quad or, \quad r^2 = \frac{I_{rms}^2}{I_{dc}^2} - 1$$

$$r = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

$$I_{avg} = I_{dc} = \frac{2I_m}{\pi} \quad and \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$r = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\boxed{r_{FWR} = 0.483}$$

Ques 3: Compare between Avalanche Breakdown and Zener Breakdown. (AKTU : 2022-23)

(2 marks)

Sol.

Parameters	Avalanche Breakdown	Zener Breakdown
Definition	The avalanche breakdown is a phenomenon of increase in e-h pairs due to carrier multiplication in reverse bias condition.	The Zener breakdown is a phenomenon of increase in e-s due to the extensive electric field in reverse bias condition.
Doping Level	Low Doping	High doping
Voltage Value	> 8V	< 6V
Junction	Destroy	Not Destroy
Electric Field	Weak	Strong
Temperature Coefficient	Positive	Negative
Ionization	Because of collision	Because of Electric Field
Breakdown Voltage	Directly proportional to temperature.	Inversely proportional to temperature.
After Breakdown	Gradual VI characteristics	Sharp VI characteristics

Ques 4.Explain the working of P-N junction diode and draw its VI Characteristics. (AKTU : 2022-23)

(7 marks)

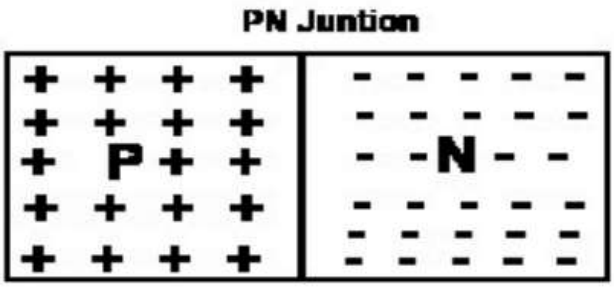
Sol.

Introduction to PN Junction Diode (Depletion Region Formation):

Diode is a device which has two terminals mainly a cathode and an anode. PN signifies the combination of p type and n type material to form it. When a p type material is joint with an n type semiconductor using a special fabrication technique, PN junction is formed.

P type material has holes as majority charge carriers. When a hole spontaneously leaves its place, a negative ion is created. So hole is represented with a compensatory –ve ion.

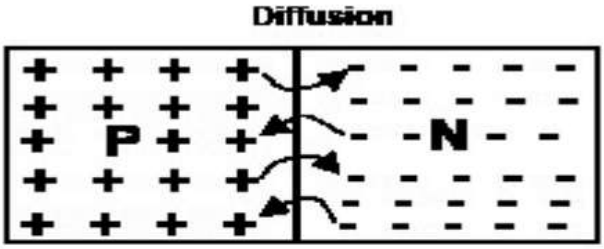
N type material has electrons as majority charge carriers. When an electron spontaneously leaves its place, a positive ion is created. So hole is represented with a compensatory +ve ion.



Depletion Region Formation

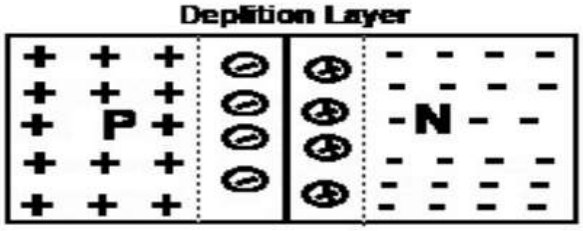
When P type material is joined with N type material, then we can see a concentration gradient (concentration difference) of charge carriers throughout whole PN junction.

The process of moving of charge carriers due to concentration gradient from higher concentration towards lower concentration spontaneously is known as Diffusion Process.



After diffusion process, negative ions are created in P side while positive ions are created in N side. Therefore an electric field is set across the junction of PN diode directed from positive ions towards negative ions. Once electric field is set up across the junction, movement of majority charge carries stop across the junction.

The region of positive and negative ions is known as depletion region. Since this region is made of space charges, this is also known as space charge region.



Potential Barrier and Barrier Potential:

Due to electric field set across the junction, A potential is also set across the junction which behaves as a barrier because it do not allow majority electrons and holes until minimum potential equal to this amount is applied to the diode.

Potential barrier is the minimum potential requirement for performing diode in ON condition. Therefore this is called Threshold voltage Cut-in voltage or Knee voltage. It is represented by V_k.

Value of Barrier Potential for Different Diodes:

We will study about the diodes made by either Si (silicon) or Ge (germanium). Both have different diode parameters.

Knee Voltage for Si diode = 0.7 Volt
Knee voltage for Ge diode = 0.3 Volt.

Working of PN Junction Diode under biasing:

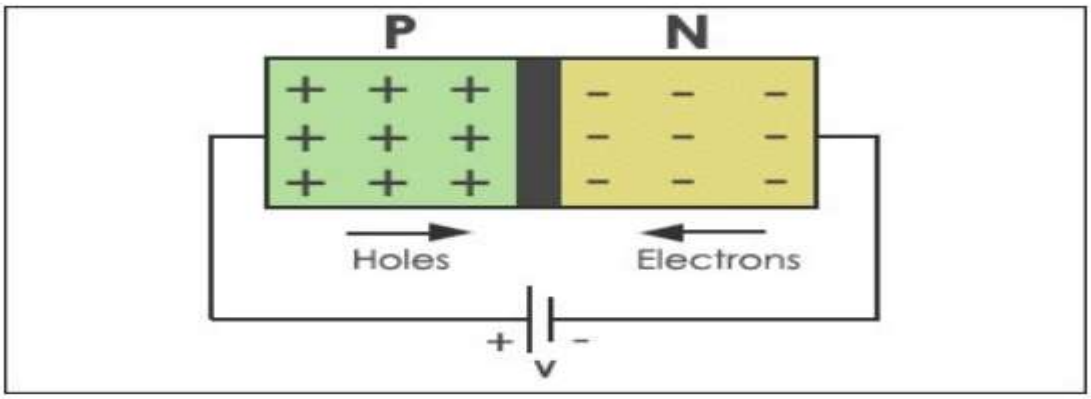
Once depletion region is formed, the diode is ready to operate voltage and current through it.

Case 1: Diode is unbiased

When diode is unbiased, no energy is provided to the electrons and holes, therefore any electrons or holes will not be able to move across the junction. **So, net current across junction will be 0 mA.**

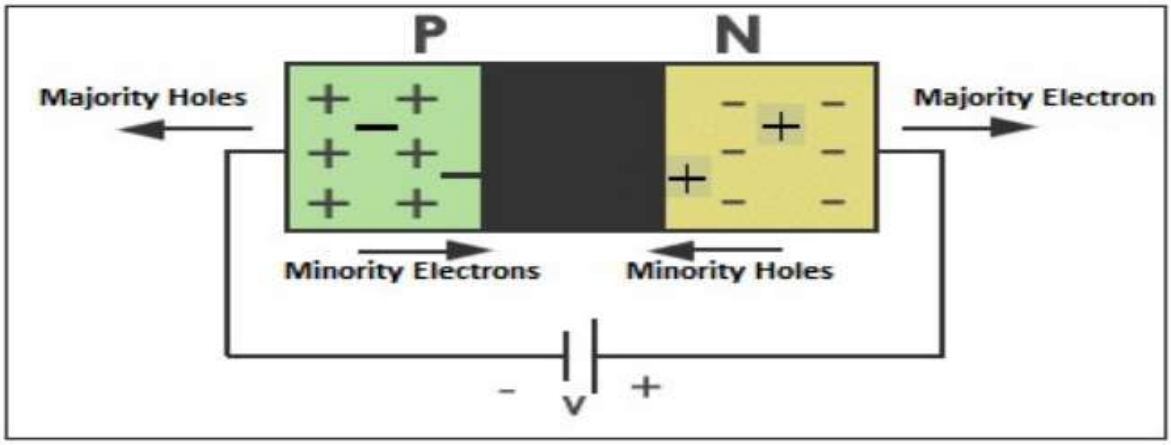
Case 2: Diode is forward bias

When Vi is positive **(Vi > 0 Volt)**, Diode is said as forward bias. We know that the junction behaves as a potential barrier with Vk voltage (knee voltage). It means diode will not allow any electron or hole movement if Vi < Vk .

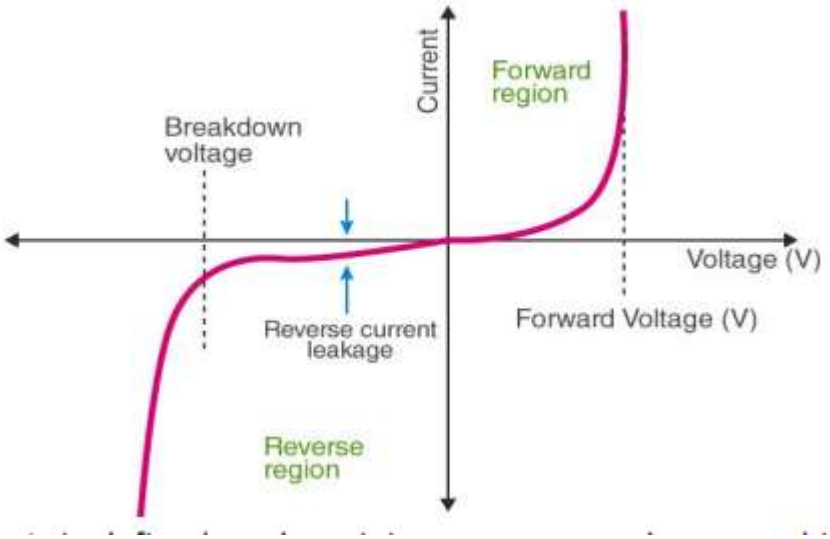


Case 3: Diode is Reverse Bias:

When Vi < 0 volt, minority charge carriers are energized to move towards the junction. Since minority charge carriers are small in numbers therefore a small current is found in the circuit. In this case, negative electrons from P side and positive holes from N side, cross the junction due to repulsion force from the battery to the minority charge carriers. Junction is wide in this case. We can see in the diagram.



VI Characteristics:



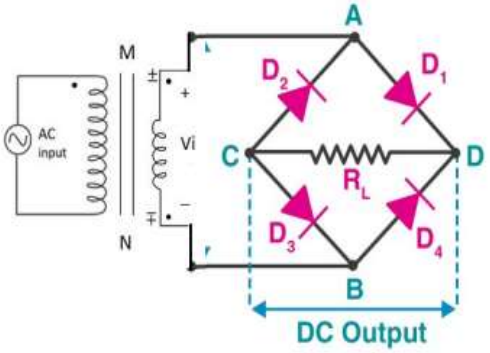
Ques 5 : Draw a neat circuit diagram of bridge rectifier and explain its operation with output waveform .Derive the average value of current and voltage. (AKTU : 2022-23)

(7 marks)

Sol.

Bridge FWR: A Bridge FWR circuit consists of 3 main parts: A transformer, A resistive load and Two diodes

A Center Tap FWR circuit diagram looks like this:



Working Analysis:

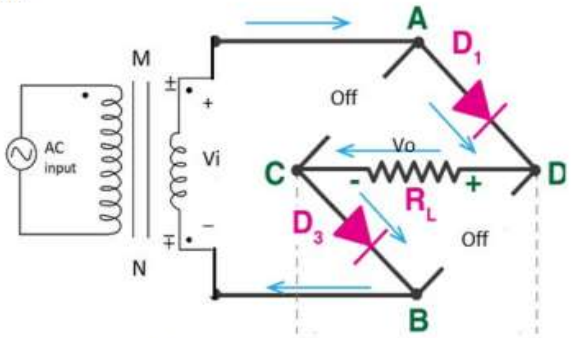
When $V_i > 2V_K$, D_1 ,D_3 is ON, D_2 ,D_4 is OFF

Drop across D_1 ,D_3 is V_K .

Applying KVL,

$$V_i - V_K - V_K - V_0 = 0$$

Or, $V_0 = V_i - 2V_K$ ---------- (i)



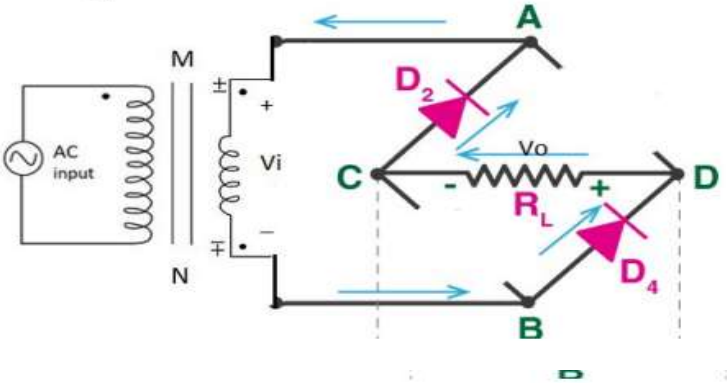
When $V_i < -2V_K$, D_1 ,D_3 is OFF, D_2 ,D_4 is OFF

Drop across D_2 ,D_4 is V_K .

Applying KVL,

$$-V_i - V_K - V_K - V_0 = 0$$

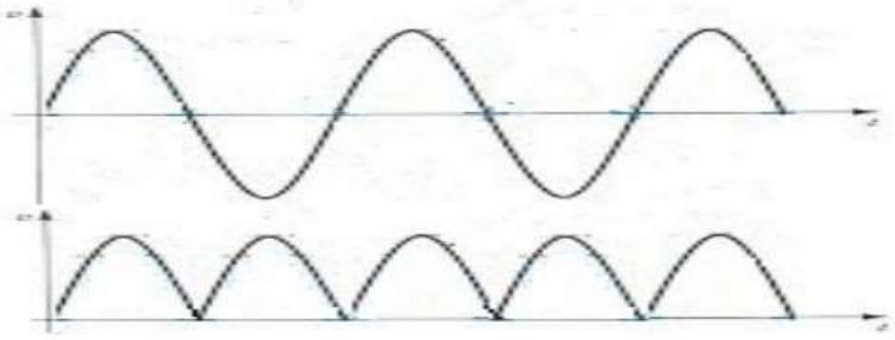
Or, $V_0 = -V_i - 2V_K$ ---------- (ii)



Output Waveform:

Case 1: when $V_i > 0$, $V_0 = V_i$

Case 2: when $V_i < 0$, $V_0 = -V_i$



Calculation of Average current and voltage:

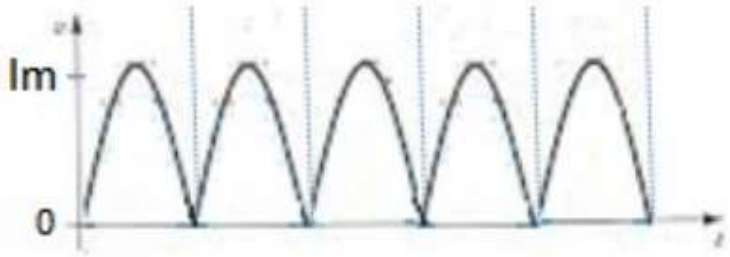
Let input voltage be

$V_i = V_m \sin(wt)$

Hence diode current is

$I(wt) = I_m \sin(wt)$ for $0 < wt < \pi$

We know that Average current can be calculate as



$$I_{avg} = I_{dc} = \frac{1}{T}\int_0^T I(wt)d(wt) \qquad where\, T = \pi$$

$$= \frac{1}{\pi}\int_0^{\pi} I(wt)d(wt) = \frac{1}{\pi}\left[\int_0^{\pi} I_m \sin(wt)d(wt)\right]$$

Calculation of RMS (Root Mean Square) current and voltage:

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2\left[\frac{1-\cos(2wt)}{2}\right]d(wt)} = \sqrt{\frac{I_m^2}{\pi}\left[\frac{1}{2}(wt)_0^{\pi} - \frac{1}{2}\left(\frac{\sin(2wt)}{2}\right)_0^{\pi}\right]}$$

$$= \sqrt{\frac{I_m^2}{\pi}\times\frac{\pi}{2}} = \sqrt{\frac{I_m^2}{2}}$$

$$V_{rms} = I_{rms}\times R_L = \frac{I_m}{\sqrt{2}}\times R_L$$

$$So, \quad V_{rms} = \frac{V_m}{\sqrt{2}(R_L + R_f)}\times R_L = \frac{V_m}{\sqrt{2}\left(1+\frac{R_f}{R_L}\right)}$$

$$But, \quad R_f << R_L \quad hence\ neglecting\ R_f$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

Ques 6 : (i) Draw the circuit diagram of voltage tripler circuit?

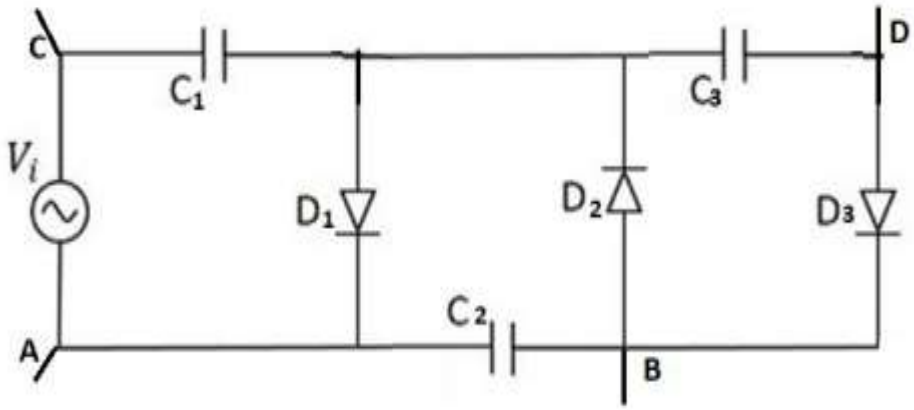
(ii) Explain Zener diode as a voltage regulator. (AKTU : 2022-23)

(7 marks)

Sol . (i) Voltage Trippler: It is an electronic circuit which produces a DC voltage equal to three times the peak value of the input voltage applied to the circuit.

$$V_{DC} = 3Vm$$

A voltage Trippler circuit is shown below. It is designed using inverse parallel combination of three diode capacitance circuits. We will start analyzing the circuit from positive half cycle where diode D1 becomes ON.



(ii)

What is a Voltage Regulator

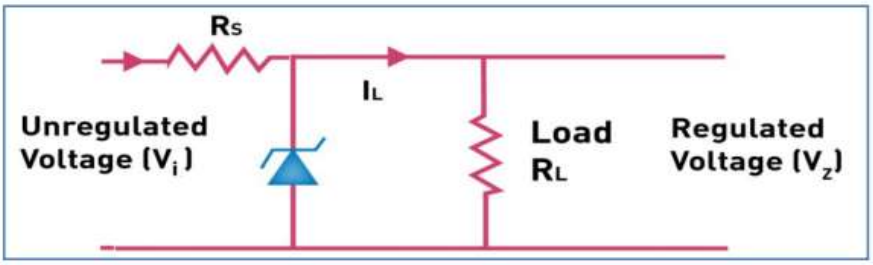
A voltage regulator is a device that regulates the voltage level. It essentially steps down the input voltage to the desired level and keeps it at that same level during the supply. This ensures that even when a load is applied the voltage doesn't drop. The voltage regulator is used for two main reasons, and they are:

1. To vary or regulate the output voltage
2. To keep the output voltage constant at the desired value in spite of variations in the supply voltage.

Voltage regulators are used in computers, power generators, alternators to control the output of the plant.

Zener Diode as a Voltage Regulator

We do not use ordinary junction diode because the low power rating diode can get damaged when we apply reverse bias above its breakdown voltage. The circuit diagram of a voltage regulator using a Zener diode is shown:



Since V_Z appears across diode when applied voltage across diode is larger than V_Z.

Therefore it is necessary to connect a series resistance in the circuit to compensate extra voltage. Due to unregulated voltage application, V_L is obtained at the load.

If $V_L > V_Z$, then V_L becomes equal to V_Z which is constant. Hence this circuit is used as voltage regulator.

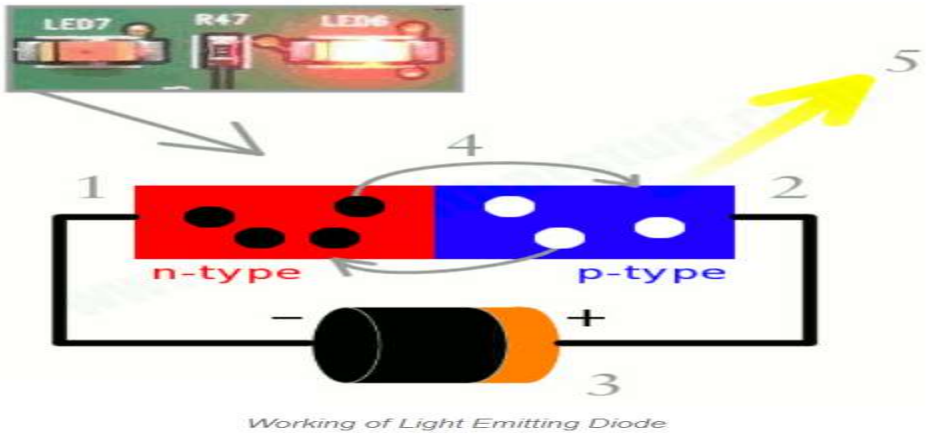
Remaining voltage is consumed by series resistance which is equal to $V_i - V_Z$.

Ques 7: Explain the working of following with the help of suitable diagram.

(i) LED

(ii) Photodiodes

Sol. LED : The Light-emitting diode is a two-lead semiconductor light source. In 1962, Nick Holonyak has come up with the idea of a light-emitting diode, and he was working for the general electric company. The LED is a special type of diode and they have similar electrical characteristics to a PN junction diode. Hence the LED allows the flow of current in the forward direction and blocks the current in the reverse direction. The LED occupies a small area which is less than **1 mm^2**. The applications of LEDs used to make various electrical and electronic projects. In this article, we will discuss the working principle of the LED and its applications.



Working of Light Emitting Diode

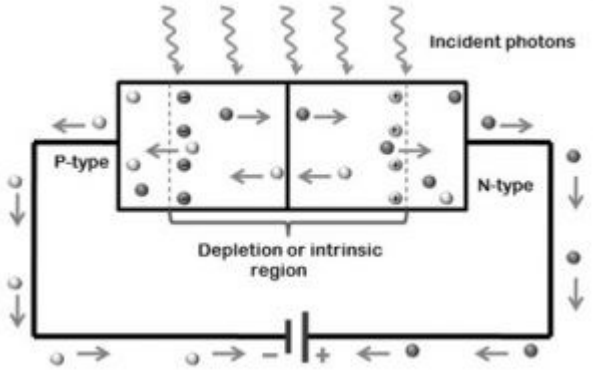
The above diagram shows how the light-emitting diode works and the step by step process of the diagram.

- From the above diagram, we can observe that the N-type silicon is in red color including the electrons which are indicated by the black circles.
- The P-type silicon is in the blue color and it contains holes, they are indicated by the white circles.
- The power supply across the p-n junction makes the diode forward biased and pushing the electrons from n-type to p-type. Pushing the holes in the opposite direction.
- Electron and holes at the junction are combined.
- The photons are given off as the electrons and holes are recombined.

(iii) Photodiodes:

A photodiode is a PN-junction diode that consumes light energy to produce an electric current. Sometimes it is also called a photo-detector, a light detector, and photo-sensor. These diodes are particularly designed to work in reverse bias conditions, it means that the P-side of the photodiode is associated with the negative terminal of the battery, and the n-side is connected to the positive terminal of the battery. This diode is very sensitive to light so when light falls on the diode it easily changes light into an electric current. The solar cell is also branded as a large-area photodiode because it converts solar energy into electric energy. Though, solar cell works only in bright light.

The working principle of a photodiode is, when a photon of ample energy strikes the diode, it makes a couple of an electron-hole. This mechanism is also called the **inner photoelectric effect.** If the absorption arises in the depletion region junction, then the carriers are removed from the junction by the inbuilt electric field of the depletion region.



Photodiode Working Principle

Therefore, holes in the region move toward the anode, and electrons move toward the cathode, and a photocurrent will be generated. The entire current through the diode is the sum of the absence of light and the photocurrent. So the absent current must be reduced to maximize the sensitivity of the device.

Ques 8: Discuss the formation of depletion layer in diode. (AKTU: 2020-21) . (2marks)

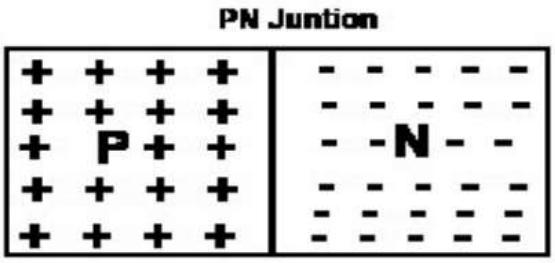
Sol.

Introduction to PN Junction Diode (Depletion Region Formation):

Diode is a device which has two terminals mainly a cathode and an anode. PN signifies the combination of p type and n type material to form it. When a p type material is joint with an n type semiconductor using a special fabrication technique, PN junction is formed.

P type material has holes as majority charge carriers. When a hole spontaneously leaves its place, a negative ion is created. So hole is represented with a compensatory –ve ion.

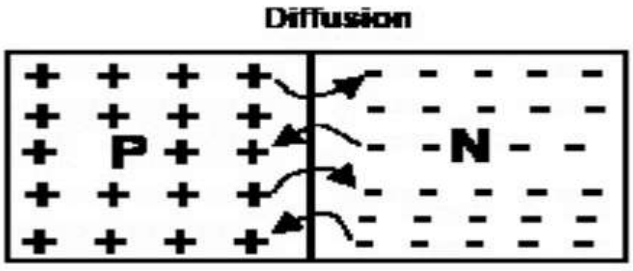
N type material has electrons as majority charge carriers. When an electron spontaneously leaves its place, a positive ion is created. So hole is represented with a compensatory +ve ion.



Depletion Region Formation

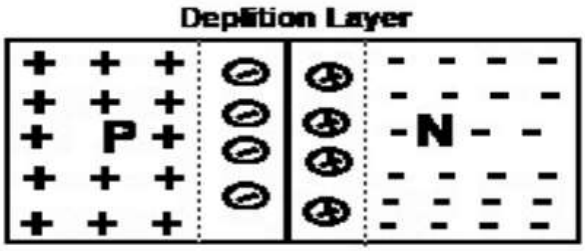
When P type material is joined with N type material, then we can see a concentration gradient (concentration difference) of charge carriers throughout whole PN junction.

The process of moving of charge carriers due to concentration gradient from higher concentration towards lower concentration spontaneously is known as Diffusion Process.



After diffusion process, negative ions are created in P side while positive ions are created in N side. Therefore an electric field is set across the junction of PN diode directed from positive ions towards negative ions. Once electric field is set up across the junction, movement of majority charge carries stop across the junction.

The region of positive and negative ions is known as depletion region. Since this region is made of space charges, this is also known as space charge region.



Potential Barrier and Barrier Potential:
Due to electric field set across the junction, A potential is also set across the junction which behaves as a barrier because it do not allow majority electrons and holes until minimum potential equal to this amount is applied to the diode.

Potential barrier is the minimum potential requirement for performing diode in ON condition. Therefore this is called Threshold voltage Cut-in voltage or Knee voltage. It is represented by V_k.

Value of Barrier Potential for Different Diodes:
We will study about the diodes made by either Si (silicon) or Ge (germanium). Both have different diode parameters.

Knee Voltage for Si diode = 0.7 Volt
Knee voltage for Ge diode = 0.3 Volt.

Ques 9 : Explain the effect of temperature on diode. (AKTU: 2020-21) . (2marks)

Sol.

Let V_{k1} be knee voltage at temperature T_1. If temperature changes to new value T_2 then knee voltage varies to new value V_{k2} as

$$V_{k2} = V_{k1} - 0.0026\,(T_2 - T_1)$$

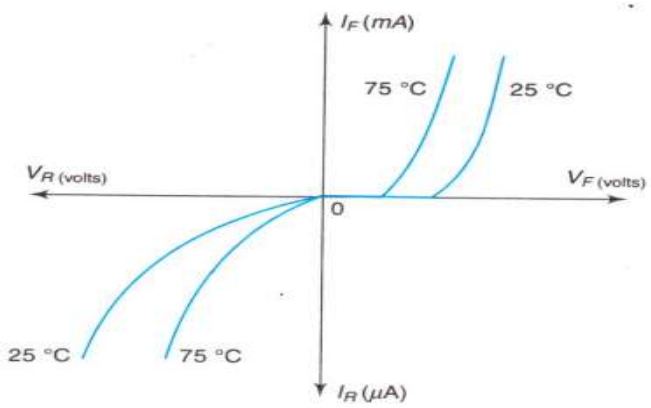
Let I_{01} be reverse saturation current at temperature T_1. If temperature changes to new value T_2 then reverse saturation current varies to new value I_{02} as

$$I_{02} = I_{01} \times 2^{\left(\frac{T_2 - T_1}{10}\right)}$$

If temperature raises by100 C, $T_2 - T_1 = 10$,

$$I_{02} = I_{01} \times 2^{\left(\frac{10}{10}\right)} = 2 \times I_{01}$$

So reverse saturation current doubles on every 10 C temperature increment.
Hence VI characteristics in different temperature statistics can be drawn as follows:



Since Knee voltage decreases and reverse saturation current increases on increasing temperature, the plot can be drawn as shown in the diagram.

Ques 10. What is doping ? What is the need of doping. (AKTU: 2020-21) . (2marks)

Sol In semiconductor production, **doping** is the intentional introduction of impurities into an intrinsic semiconductor for the purpose of modulating its electrical, optical and structural properties. The doped material is referred to as an extrinsic semiconductor.

Small numbers of dopant atoms can change the ability of a semiconductor to conduct electricity. When on the order of one dopant atom is added per 100 million atoms, the doping is said to be *low* or *light*. When many more dopant atoms are added, on the order of one per ten thousand atoms, the doping is referred to as *high* or *heavy*. This is often shown as *n+* for n-type doping or *p+* for p-type doping.

In general, increased doping leads to increased conductivity due to the higher concentration of carriers. Degenerate (very highly doped) semiconductors have conductivity levels comparable to metals and are often used in integrated circuits as a replacement for metal. Often superscript plus and minus symbols are used to denote relative doping concentration in semiconductors. For example, n^+ denotes an n-type semiconductor with a high, often degenerate, doping concentration. Similarly, p^- would indicate a very lightly doped p-type material.

Ques 11 : Define voltage multiplier. Draw the circuit and explain the working of voltage tripler and quadrupler circuit. (AKTU: 2020-21) . (10 marks)

Sol.

Voltage Multiplier-

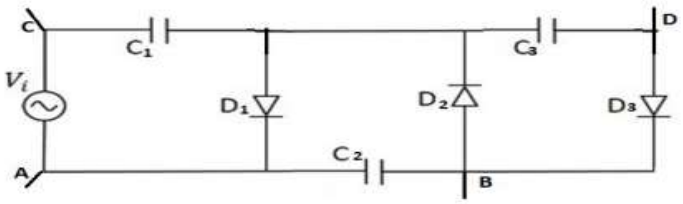
Voltage Doubler: It is an electronic circuit which produces a DC voltage equal to Two times the peak value of the input voltage applied to the circuit. $V_{DC} = 2V_m$

There are two types of voltage doubler circuits:
1 – Half Wave Doubler, 2 – Full Wave Doubler

Voltage Trippler: It is an electronic circuit which produces a DC voltage equal to three times the peak value of the input voltage applied to the circuit. $V_{DC} = 3V_m$

A voltage Trippler circuit is shown below. It is designed using inverse parallel combination of three diode capacitance circuits.

We will start analyzing the circuit from positive half cycle where diode D_1 becomes ON.



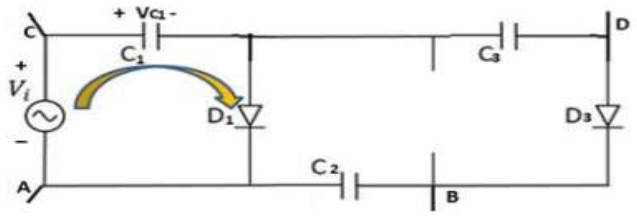
Analysis: For first positive half cycle ($V_i > 0$), D_1 and D_3 diodes are ON but capacitor will charge only through diode D_1 because D_1 is low resistance path while $C_3 - D_3$ is high impedance path.

At the same time diodes D_2 is OFF.

Applying KVL, $V_i - V_{C1} = 0$ or $V_{C1} = V_i|_{max}$

Or, $\mathbf{V_{C1} = V_m}$

After C_1 is charged up to $V_C = V_m$, diode D_1 will never be ON again



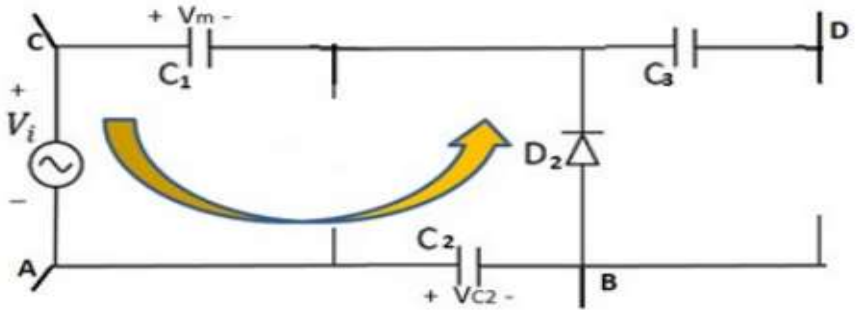
For first negative half cycle ($V_i < 0$), D_2 is ON.

At the same time diodes D_1 and D_3 are OFF.

Applying KVL, $-V_i - V_{C2} + V_m = 0$ or $V_{C2} = -V_i|_{max} + V_m$

Or, $\mathbf{V_{C2} = V_m + V_m = 2V_m}$

After C_2 is charged up to $V_{C2} = 2V_m$, diode D_2 will never be ON again.

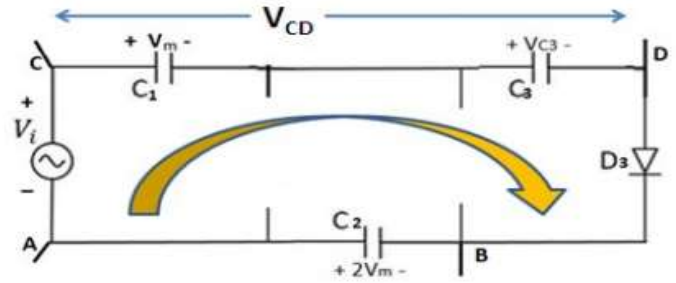


For next positive half cycle ($V_i > 0$), D_3 diodes are ON only because D_1 and D_2 are already OFF.

Applying KVL, $V_i - V_m - V_{C3} + 2V_m = 0$ or $V_{C3} = V_i|_{max} - V_m + 2V_m$

Or, $\mathbf{V_{C3} = V_m - V_m + 2V_m = 2V_m}$

After C_3 is charged up to $V_{C3} = 2V_m$, diode D_3 will never be ON again.



Hence $V_{CD} = V_{C1} + V_{C3} = V_m + 2V_m$ or $\mathbf{V_{CD} = 3V_m}$ **(Trippler)**

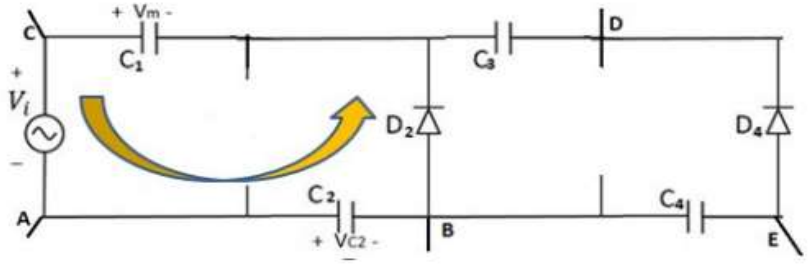
Voltage Quadrupler: Analysis: For first negative half cycle ($V_i < 0$), D_2 and D_4 diodes are ON but capacitor will charge only through diode D_2 because D_2 is low resistance path while $C_4 - D_4$ is high impedance path.

At the same time diodes D_1 and D_3 are OFF.

Applying KVL, $-V_i - V_{C2} + V_m = 0$ or $V_{C2} = -V_i\,|_{max} + V_m$

Or, $\mathbf{V_{C2} = V_m + V_m = 2V_m}$

After C_2 is charged up to $V_{C2} = 2V_m$, diode D_2 will never be ON again.



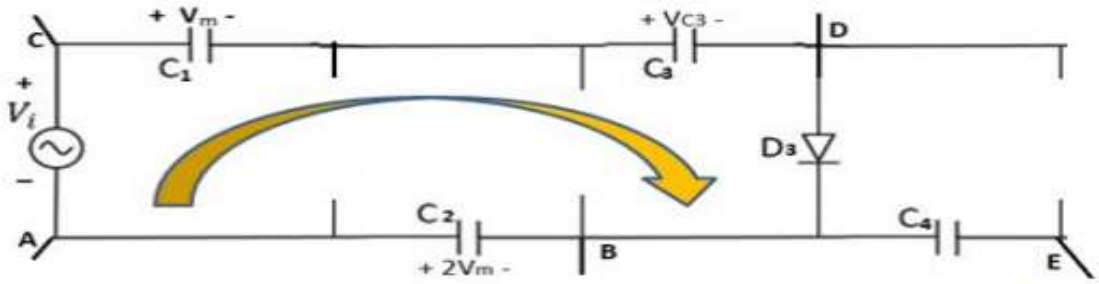
For next positive half cycle ($V_i > 0$), D_3 diodes are ON only because D_1 is already OFF.

At the same time diodes D_2 and D_4 are also OFF.

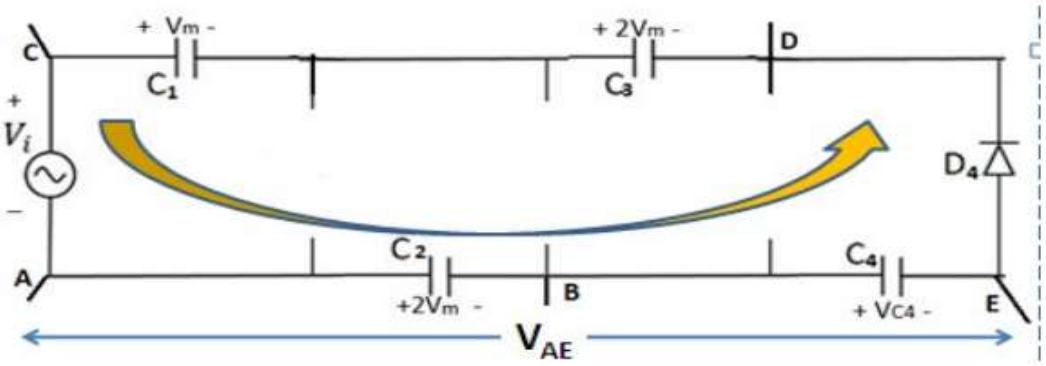
Applying KVL, $V_i - V_m - V_{C3} + 2V_m = 0$ or $V_{C3} = V_i\,|_{max} - V_m + 2V_m$

Or, $\mathbf{V_{C3} = V_m - V_m + 2V_m = 2V_m}$

After C_3 is charged up to $V_{C3} = 2V_m$, diode D_3 will never be ON again.



For next negative half cycle ($V_i < 0$), D_4 diodes are ON only because D_2 is already OFF.
At the same time diodes D_1 and D_3 are also OFF.
Applying KVL, $-V_i - 2V_m - V_{C4} + 2V_m + V_m = 0$ or $V_{C4} = -V_i|_{max} + V_m$
Or, $\mathbf{V_{C4} = V_m + V_m = 2V_m}$
After C_4 is charged up to $V_{C4} = 2V_m$, diode D_4 will never be ON again.



Hence $V_{AE} = V_{C2} + V_{C4} = 2V_m + 2V_m$ or $\mathbf{V_{AE} = 4V_m}$

Ques 12: Draw the VI characteristics of an ideal diode in forward and reverse bias conditions.

(AKTU: 2020-21) . (2 marks)

Sol.

Ideal VI Characteristics

An ideal VI characteristic of a diode is shown in the diagram. This was the assumption about the correct usefulness of a diode. According to this concept, (1) For VD > 0, diode becomes immediately ON and current tends towards infinite value, (2) For VD < 0, diode becomes immediately OFF and current becomes absolutely zero.

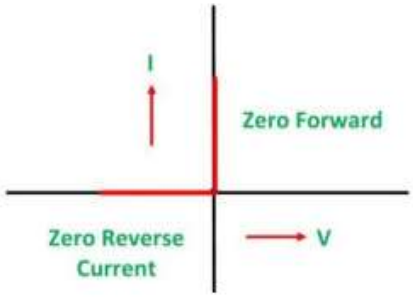
As diode voltage VD tends to 0+, current tends to its maximum value

So forward resistance $Rf = V_D / I = 0 / I = 0\ \Omega$ (Short Circuit)

As diode voltage becomes 0 or 0- , current also becomes 0.

So reverse resistance $Rr = V_D / I = V_D / 0 = \infty\ \Omega$ (Open Circuit)

We always approach to fabricate a diode which has parameters very close to the Ideal diode. It is not possible to design an ideal diode.



Ques 13. Why bridge type full wave rectifier is preferred over center tapped full wave rectifier. State two reasons. (AKTU: 2020-21) . (2 marks)

Sol. 1.The efficiency of the bridge rectifier is higher than the efficiency of a half-wave rectifier. However, the rectifier efficiency of the bridge rectifier and the center-tapped full-wave rectifier is the same.

2.The DC output signal of the bridge rectifier is smoother than the output DC signal of a center-tapped full-wave rectifier.

Ques 14. Define the term ripple factor. What is the value of the ripple factor for a half wave rectifier and a full wave rectifier? (AKTU: 2020-21) . (4 marks)

Sol.

Calculation of Ripple Factor (r): Ripple is defined as unwanted ac component present in the DC ou of rectifier circuit. Ripple factor is defined as the ratio of ac component to DC output.

We know that

$$I_{rms}^2 = I_{ac}^2 + I_{dc}^2 \quad or, \quad I_{ac}^2 = I_{rms}^2 - I_{dc}^2, \quad devide equation by I_{dc}^2$$

$$\frac{I_{ac}^2}{I_{dc}^2} = \frac{I_{rms}^2}{I_{dc}^2} - 1 \quad or, \quad r^2 = \frac{I_{rms}^2}{I_{dc}^2} - 1$$

$$r = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

$$I_{avg} = I_{dc} = \frac{I_m}{\pi} \quad and \quad I_{rms} = \frac{I_m}{2}$$

$$r = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1}$$

$$\boxed{r_{HWR} = 1.21}$$

Calculation of Ripple Factor (r): Ripple is defined as unwanted ac component present in the DC output of rectifier circuit. Ripple factor is defined as the ratio of ac component to DC output.

We know that

$$I_{rms}^2 = I_{ac}^2 + I_{dc}^2 \quad or, \quad I_{ac}^2 = I_{rms}^2 - I_{dc}^2, \quad devide\ equation\ by\ I_{dc}^2$$

$$\frac{I_{ac}^2}{I_{dc}^2} = \frac{I_{rms}^2}{I_{dc}^2} - 1 \quad or, \quad r^2 = \frac{I_{rms}^2}{I_{dc}^2} - 1$$

$$r = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

$$I_{avg} = I_{dc} = \frac{2I_m}{\pi} \quad and \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$r = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\boxed{r_{FWR} = 0.483}$$

Ques 15: With help of a neat diagram, explain the working of a voltage doubler circuit.

(AKTU: 2020-21) . (6 marks)

Sol.

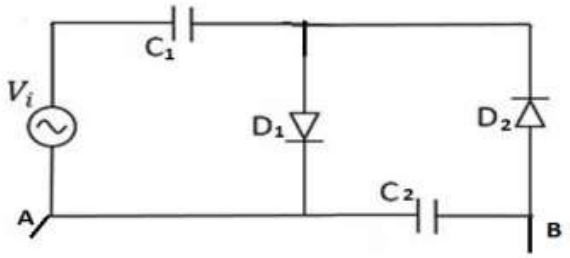
Voltage Multiplier-

Voltage Doubler: It is an electronic circuit which produces a DC voltage equal to Two times the peak value of the input voltage applied to the circuit. $V_{DC} = 2V_m$

There are two types of voltage doubler circuits:

1 – Half Wave Doubler, 2 – Full Wave Doubler

1 – Half Wave Voltage doubler: A Half wave voltage doubler circuit is shown below. It is designed using inverse parallel combination of two diode capacitance circuits. We will start analyzing the circuit from positive half cycle where diode D_1 becomes ON.



Voltage Doubler: Half Wave Voltage doubler:

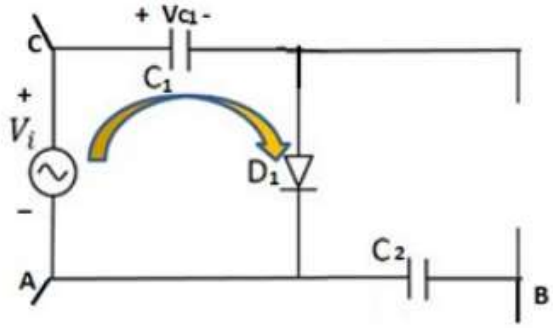
Analysis: For positive half cycle ($V_i > 0$), D_1 diode is ON.

At the same time diodes D_2 is OFF.

Applying KVL, $V_i - V_{C1} = 0$ or $V_{C1} = V_i|_{max}$

Or, $\mathbf{V_{C1} = V_m}$

After C_1 is charged up to $V_C = V_m$, diode D_1 will never be ON again.



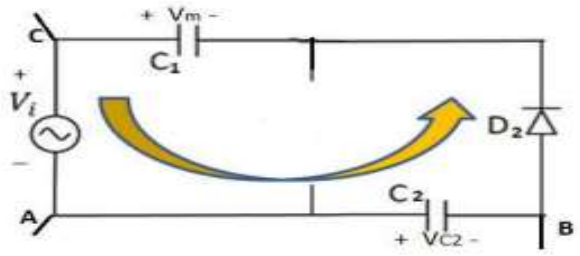
For negative half cycle ($V_i < 0$), D_2 is ON.

At the same time diodes D_1 is OFF.

Applying KVL, $-V_i - V_{C2} + V_m = 0$ or $V_{C2} = -V_i|_{max} + V_m$

Or, $\mathbf{V_{C2} = -(-V_m) + V_m}$ $\mathbf{V_{C2} = V_m + V_m = 2V_m}$

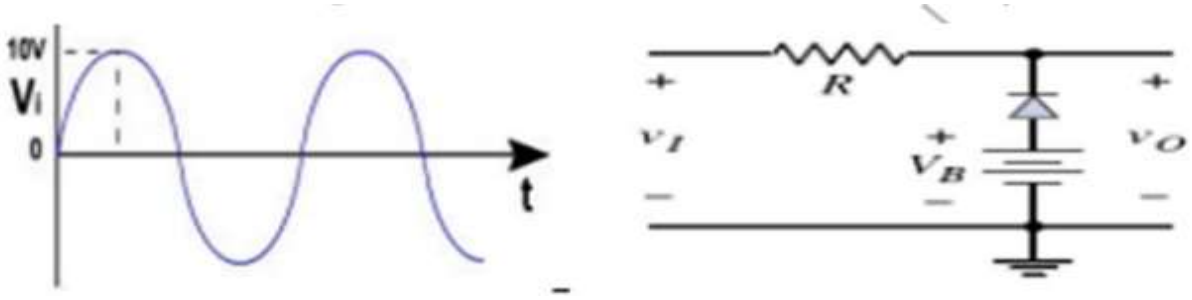
After C_2 is charged up to $V_{C2} = 2V_m$, diode D_2 will never be ON again.



Output voltage

$\mathbf{V_{AB} = V_{C2} = 2V_m}$ **(Doubler)**

Ques 16: What do mean by clipper? Draw the output waveform of given circuits.

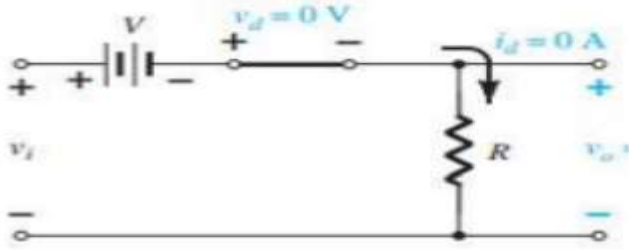


(AKTU: 2020-21) . (10 marks)

Sol.

Input is in series with diode so it is called series clipper.

When Vi > V, diode is ON. Replace diode with short circuit equivalent and apply KVL

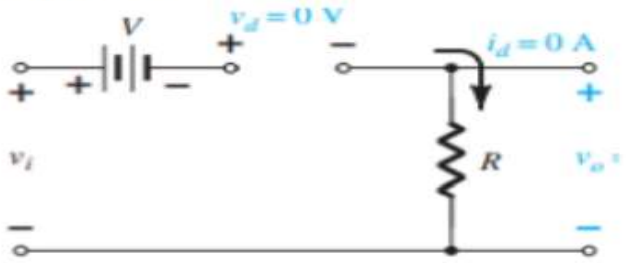


KVL in above loop

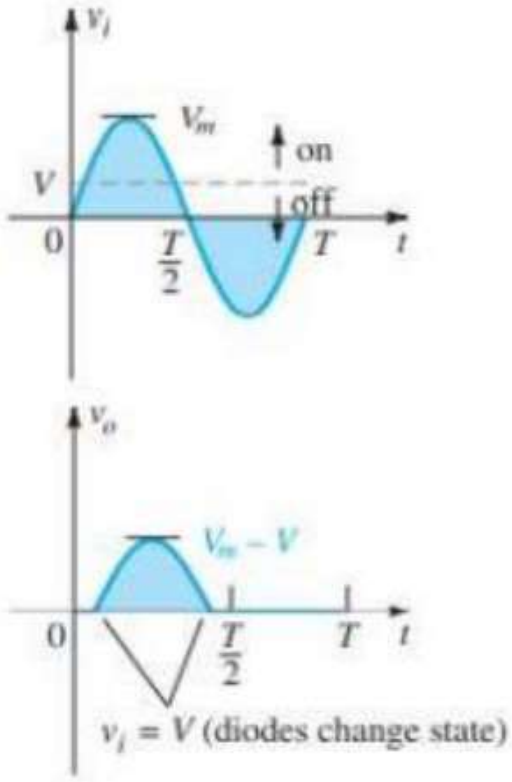
$Vi - V - Vo = 0$

So $Vo = (Vi - V)$

When $Vi < V$, diode is ON. Replace diode with open circuit equivalent and apply KVL



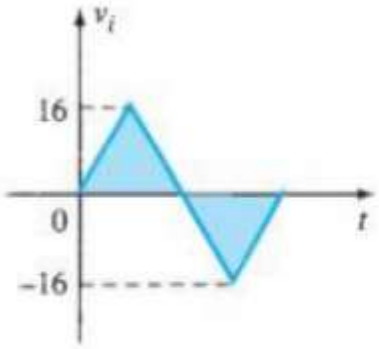
Current is zero so $Vo = 0$

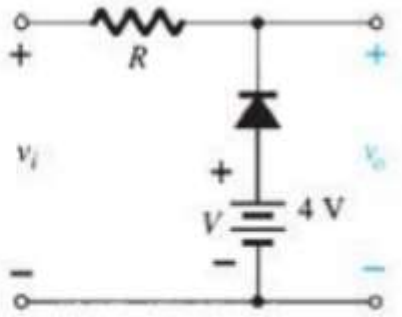


Certain portion of input is clipped by this circuit.

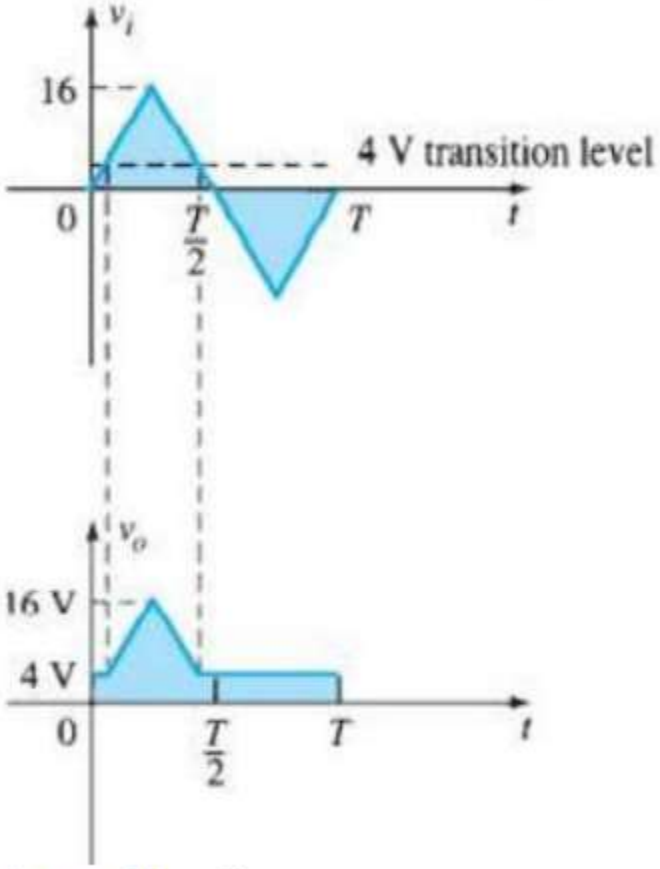
Parallel Clipper

Input is in parallel with diode so these types of clippers are called parallel clipper or shunt clipper.

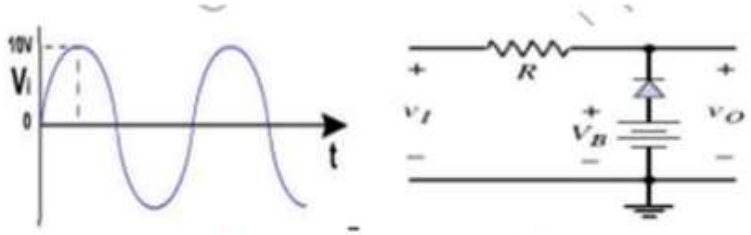




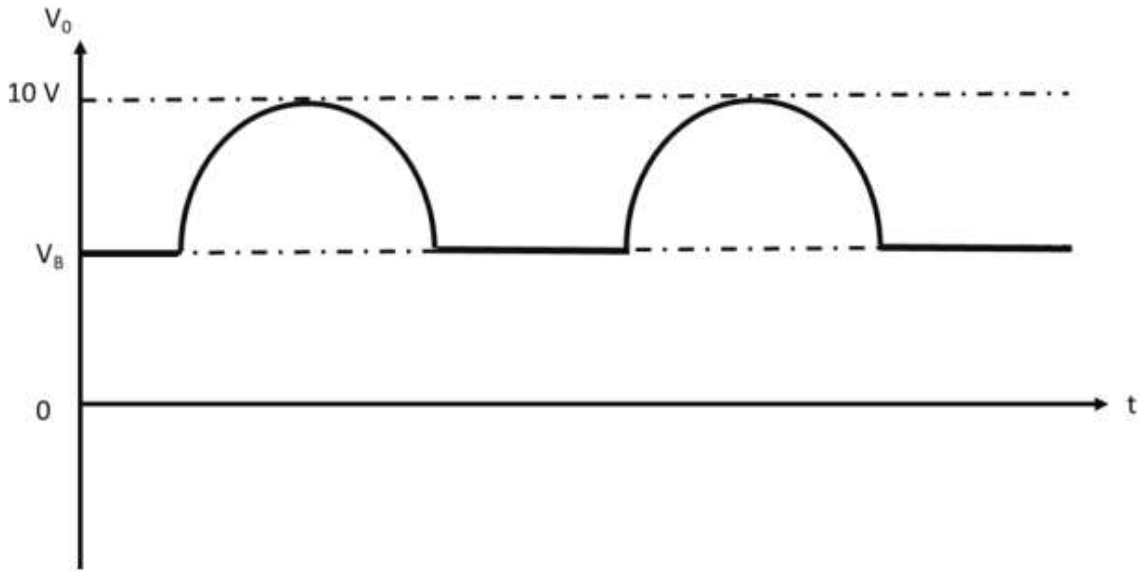
Input Waveform



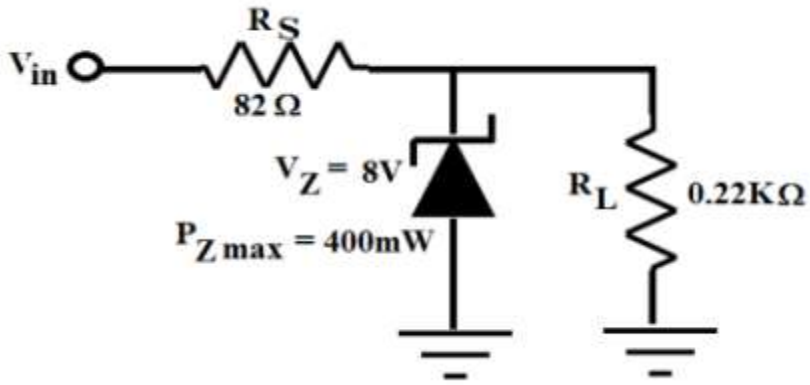
Output Waveform



Let us assume that $V_B = 5$ V i.e $V_B < 10$ V.



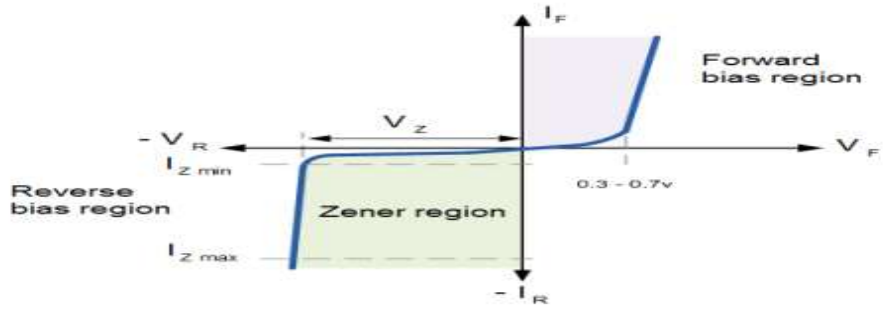
Ques 17: Draw the V-I characteristics of zener diode. Determine the network of figure given below, determine the range of Vin that will maintain VL at 8V and not exceeded the maximum power rating.



(AKTU: 2020-21) . (10 marks)

Sol.

Zener Diode is a reverse-biased heavily-doped PN junction diode which operates in the breakdown region. The reverse breakdown of a PN- junction may occur either due to Zener effect or avalanche effect. Zener effect dominates at reverse voltages less than 5 volt whereas avalanche effect dominates above 5 V. Hence, first one should be called Zener diode. But for simplicity, both types are called Zener Diodes. The breakdown voltage of a Zener diode can be set by controlling the doping level. For Zener diodes, silicon is preferred to Ge because of its high temperature and current capability. This post includes explanation of operation of Zener diode and V-I Characteristics of Zener Diode.



NUMERICAL SOLUTION

for max:

3(b) $\frac{V_{in} - 8}{82} = 50\,mA + \left(\frac{8}{0.22}\right) mA$

$\frac{V_{in})_{max} - 8}{82} = 86.36\,mA$

$V_{in})_{max} \simeq 15.081$

$V_{in})_{max} \simeq 15\ V$

$\frac{V_{in})_{min} - 8}{82} = \left(\frac{8}{0.22}\right) mA$

$V_{in})_{min} \simeq 10.981\ V$

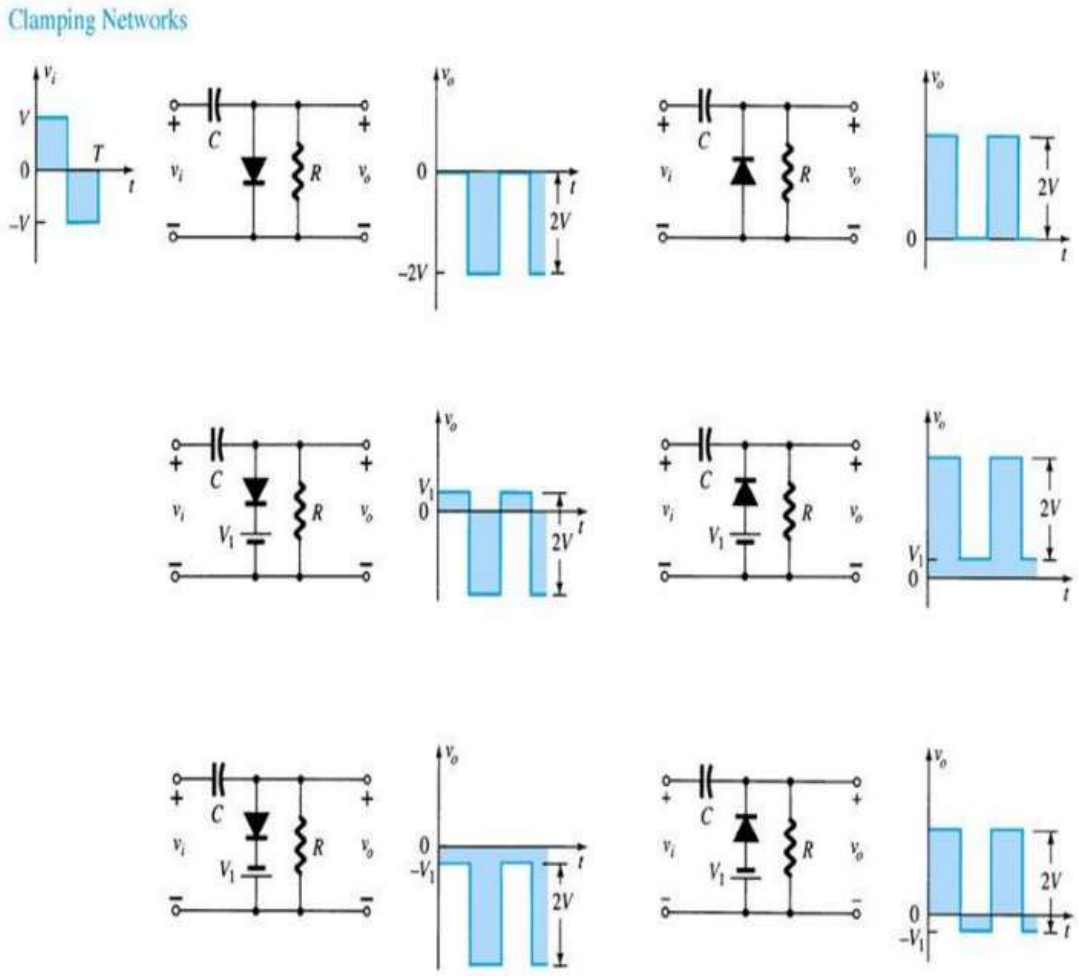
$V_{in})_{min} \simeq 11\ V$

Ans: $[V_{in} = (11 - 15)V]$.

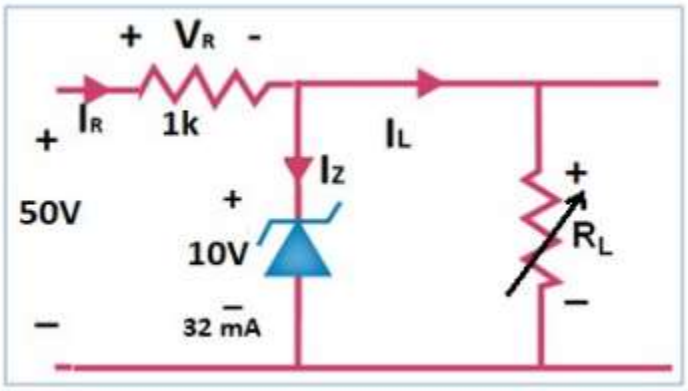
Ques 18. Explain Positive and Negative Clamper using suitable circuit diagram and input/output waveform. (AKTU:2020-21) (5 marks)

Sol. A clamper is an electronic circuit that changes the DC level of a signal to the desired level without changing the shape of the applied signal. In other words, the clamper circuit moves the whole signal up or down to set either the positive peak or negative peak of the signal at the desired level.

The dc component is simply added to the input signal or subtracted from the input signal. A clamper circuit adds the positive dc component to the input signal to push it to the positive side. Similarly, a clamper circuit adds the negative dc component to the input signal to push it to the negative side.



Ques 19. For the network of figure, determine the range of RL and IL that will result in VRL being maintained at 10V. Also calculate maximum wattage rating of diode.



Solution: $V_L = V_Z = 10V$, $I_{ZM} = 32$ mA

$R_S = 1\ k\Omega$, and $V_i = 50V$

Now, $\mathbf{R_{L,min} = V_Z R_S / (V_i - V_Z)}$

$= 10 \times 1/(50 - 10) = ¼ = 0.25\ k\Omega$

Now, $I_{L,max} = V_Z/R_{L,min} = 10/0.25 = 40$ mA

So $R_{L,min} = 0.25k\Omega$ and $I_{L,max} = 40$ mA

Now $I_R = V_R/R_S = (50 - 10)/1 = 40$ mA

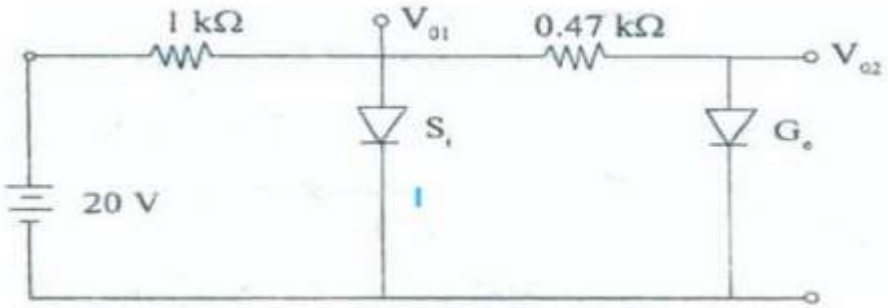
So $I_{L,min} = I_R - I_{ZM} = 40 - 32 = 8$ mA

And $R_{L,max} = V_Z / I_{L,min} = 10V / 8mA = 1.25\ k\Omega$

So $R_{L,max} = 1.25k\Omega$ and $I_{L,min} = 8$ mA

Answer: Range of R_L = 0.25 to 1.25 kΩ **and Range of I_L** = 8 mA to 40 mA

Ques 20. Determine V01, V02 and I for the network of Figure



Solution: Both the diodes are ON

So, V_{01} = drop across Si diode

= 0.7 V

V_{02} = drop across Ge diode

= 0.3 V

Current in Ge diode = $(V_{01} - V_{02})/0.47$ mA

= $(0.7 - 0.3)/0.47$ mA = 0.4 / 0.47 mA = 0.851 mA

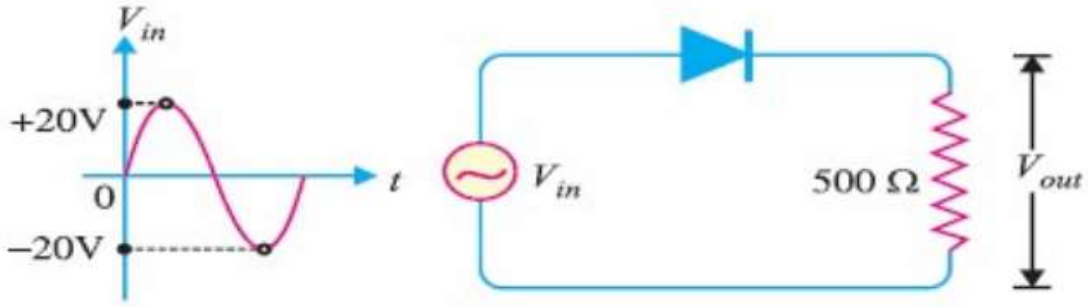
Current in source = $(V_{in} - V_{01})/1$ mA = $20 - 0.7$ = 19.3 mA

So, Current I = Current in source − Current in Ge Diode

= $19.3 - 0.851 = 18.449$ = **18.45 mA**

Ques 21: An a.c. voltage of peak value 20 V is connected in series with a silicon diode and load resistance of 500 Ω. If the forward resistance of diode is 10 Ω, find : (i) peak current through diode (ii) peak output voltage What will be these values if the diode is assumed to be ideal.

Solution: According to the question, the circuit can be drawn as follows



Solution: Diode will be ON in positive half cycle ($V_{in} > 0$)

Diode will be OFF in negative half cycle ($V_{in} < 0$)

Peak input voltage V_p = 20 V (Diode is ON here)

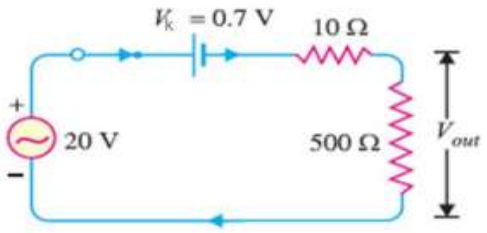
Forward resistance, r_f = 10 Ω

Load resistance, R_L = 500 Ω

Potential barrier voltage, V_k = 0.7 V

The diode will conduct during the positive half-cycles of a.c. input voltage only.

The equivalent circuit is shown as,



The peak current through the diode will occur at the instant when the input voltage reaches positive peak i.e. Vin=V_p =20 V

$$V_p - V_k - (I_f)_{peak}\, r_f - (I_f)_{peak}\, R_L = 0$$

$$(I_f)_{peak}\,[r_f + R_L] = V_p - V_k$$

$$(I_f)_{peak} = \frac{V_p - V_k}{r_f + R_L} = \frac{20 - 0.7}{10 + 500} = \frac{19.3}{510}\ \text{A} = \mathbf{37.8\ mA}$$

Peak output voltage:

$$\text{Peak output voltage} = (I_f)_{peak} \times R_L$$

$$= 37.8\ \text{mA} \times 500\ \Omega = \mathbf{18.9\ V}$$

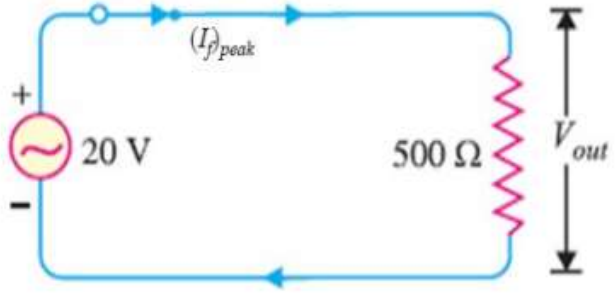
(i) The peak current through the diode will occur at the instant when the input voltage reaches positive peak i.e. Vin=V_p =20 V

Ideally V_k = 0 and R_f = 0 (Short Circuit)

Applying KVL $V_P - V_{out} = 0$

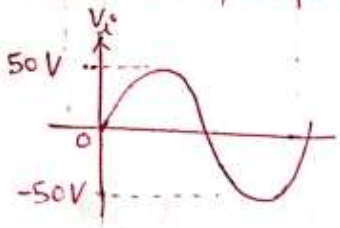
$V_{out} = V_P$ = 20 V

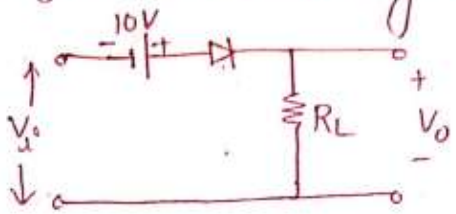
And $(I_f)_{peak}$ = 20 / 500 = 40 mA



Numerical on Clipper Circuits

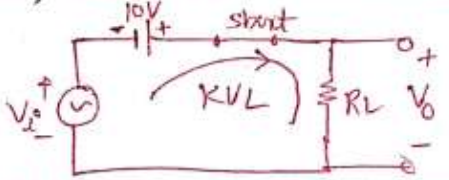
Q: Sketch the output for the given circuit assuming diode is ideal,





Solution: $V_i = +10$ is applied to the p-side so,

if $V_i + 10 > 0$ or $V_i > -10V$, diode is ON, so short circuit.



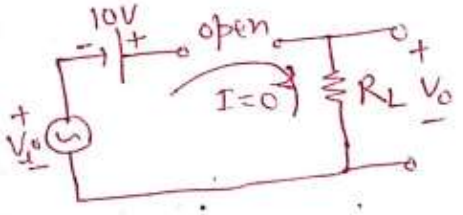
So applying KVL

$V_i + 10 - V_o = 0$

or $V_o = V_i + 10$

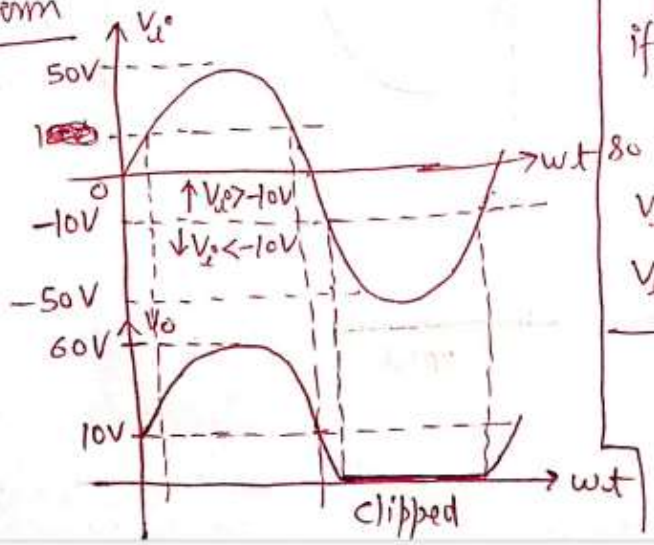
So **if $V_i > -10V$, $V_o = V_i + 10$**

if $V_i < -10V$, diode is OFF hence open circuit. So current in the circuit $I = 0$



So, **if $V_i < -10V$, $V_o = 0$**

Output Waveform



if $V_i < -10V$ $V_o = 0$

if $V_i > -10V$,
$V_o = V_i + 10$

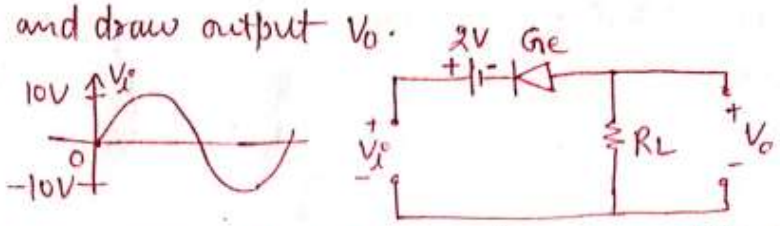
So $V_i = 0$ $V_o = 10V$

$V_i = 50$, $V_o = 60V$

$V_i = -10V$, $V_o = 0V$

[PTO]

Q: Calculate and draw output V_0.

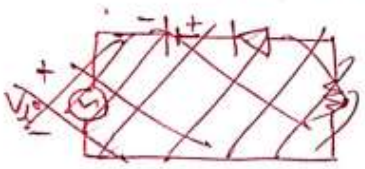


Solution: 0V is applied at p-side and $V_i - 2$ is applied at n-side

So $0 - (V_i - 2) > 0.3$ where 0.3V is knee voltage

or $-V_i + 2 > 0.3$

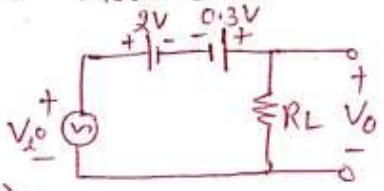
or $-V_i > -1.7V$ or $V_i < 1.7V$ Diode is ON



Applying KVL,

$V_i - 2 + 0.3 - V_0 = 0$

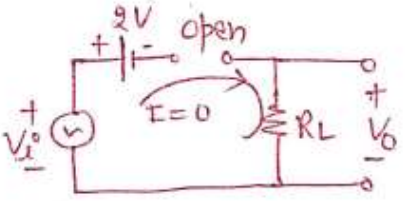
or $\boxed{V_0 = V_i - 1.7V}$ (for $V_i < 1.7V$)



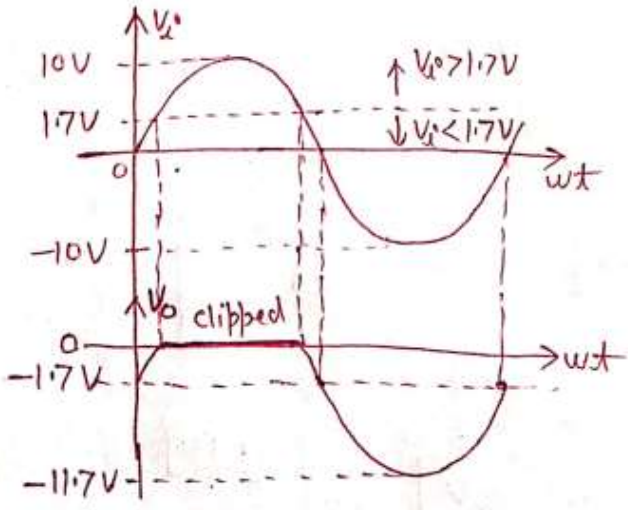
if $V_i > 1.7V$, diode is off, open hence current in circuit $I = 0$

hence $V_0 = I \times R_L = 0$

or $\boxed{V_0 = 0}$ (for $V_i > 1.7V$)



Output Waveform:



if $V_i > 1.7V$ $V_0 = 0$

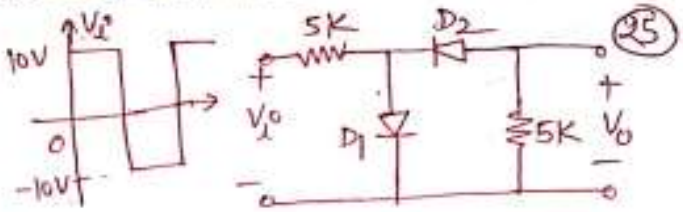
if $V_i < 1.7V$ $V_0 = V_i - 1.7V$

$V_i = 1.7V$ $V_0 = 0$

$V_i = 0$ $V_0 = -1.7V$

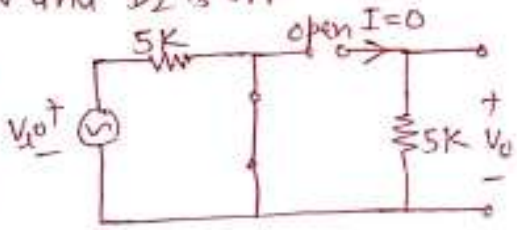
$V_i = -10V$ $V_0 = -11.7V$

Q: Sketch output voltage V_o for the circuit shown. Assume ideal diodes.



Soln: if $V_i > 0$ or $V_i = 10V$, D_1 is ON and D_2 is off

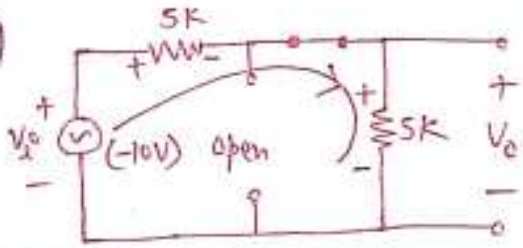
Since D_2 is open, so current in the output circuit $I = 0$



So output voltage $V_o = IR = 0$

So **if $V_i = 10V$, $V_o = 0$**

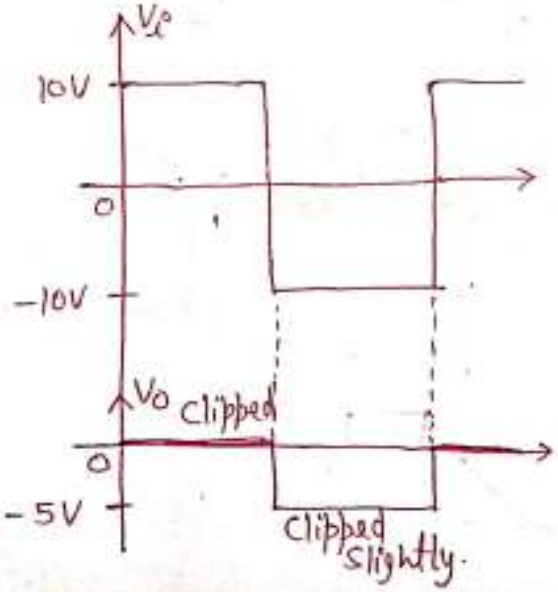
if $V_i < 0$ or $V_i = -10V$, D_1 is off and D_2 is ON. So output voltage can be found by applying potential division rule as,



$$V_o = \frac{V_i \times 5}{5+5} = \frac{V_i}{2}$$

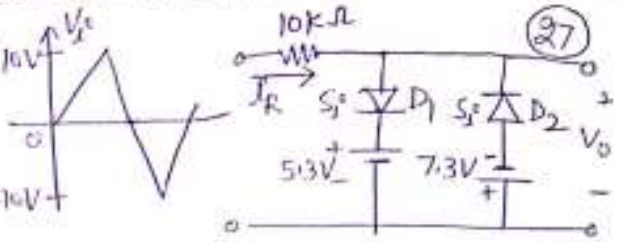
or $$V_o = \frac{-10}{2} = -5V$$

So if $V_i = -10V$, $V_o = -5V$



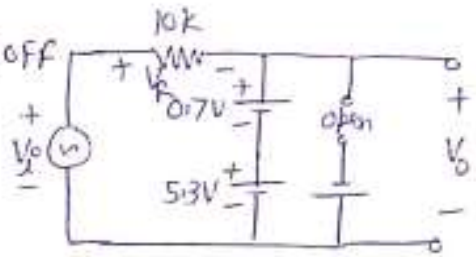
if $V_i = 10V$, $V_o = 0$
if $V_i = -10V$, $V_o = -5V$

Q: Sketch i_R and V_o for the network shown in figure.



Solution: (a) if $V_i - 5.3V > 0.7V$

or $V_i > 6V$, D_1 is ON, D_2 is OFF



so $V_{D_1} = 0.7V$ and D_2 is open.

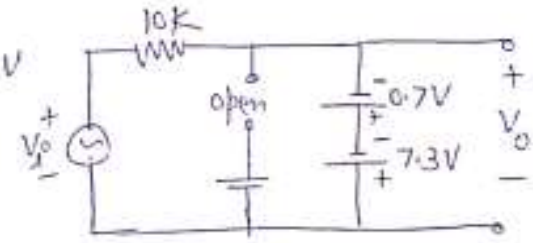
so $V_o = 0.7 + 5.3 = 6V$

so **if $V_i > 6V$, $V_o = 6V$**

so, $i_R = \frac{V_R}{10} = \frac{V_i - 6}{10}$ mA or **$i_R = \frac{V_i - 6}{10}$ mA**

(b) if $0 - 7.3V - V_i > 0.7V$ or $V_i < -8V$

D_1 is OFF and D_2 is ON



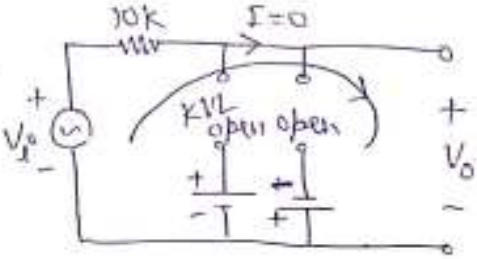
so $V_{D_2} = 0.7V$ and D_1 is open.

so $V_o = -0.7 - 7.3 = -8V$

so **if $V_i < -8V$, $V_o = -8V$**

so $i_R = \frac{V_i - (-8)}{10} = \frac{V_i + 8}{10}$ mA or **$i_R = \frac{V_i + 8}{10}$ mA**

(c) if $-8V < V_i < 6V$, diodes D_1 and D_2 are off, so circuit is open and current $I = 0$



so applying KVL, $V_i - IR - V_o = 0$

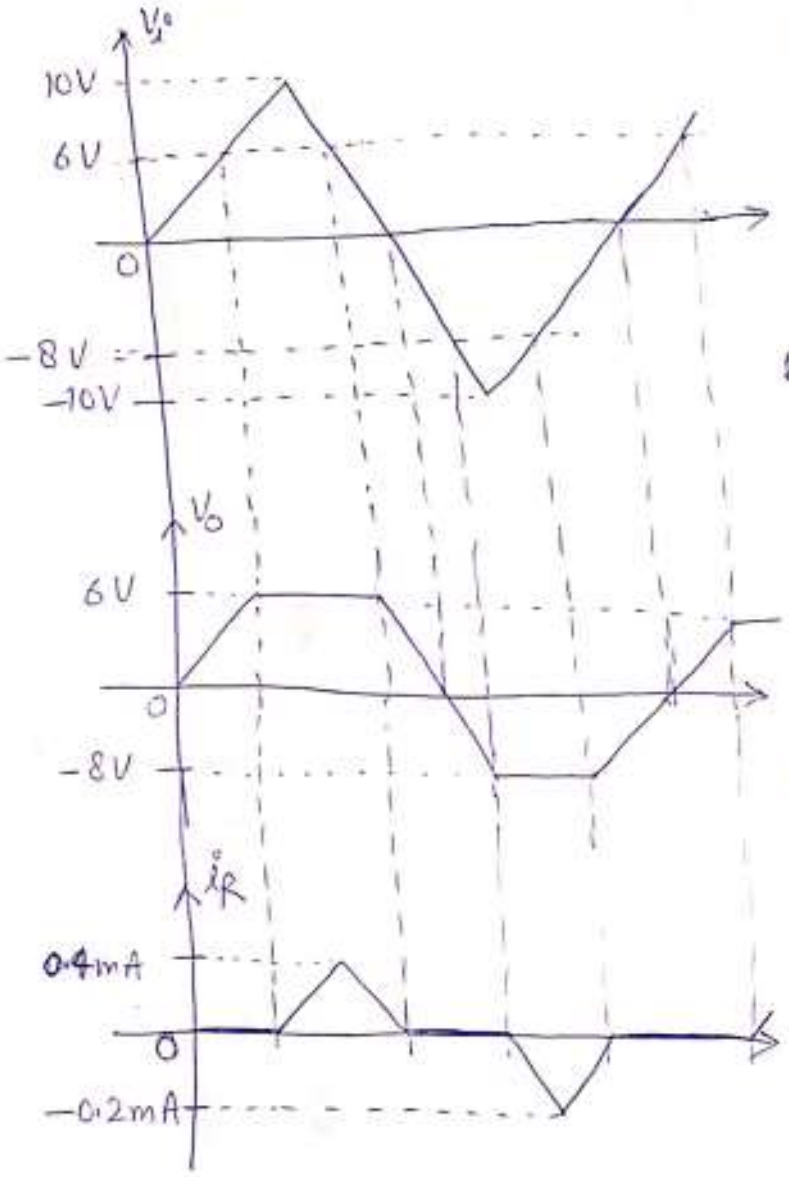
or $V_o = V_i$

so **if $-8V < V_i < 6V$, $V_o = V_i$**

$i_R = \frac{V_i - V_o}{10} = \frac{V_i - V_i}{10} = 0$ or **$i_R = 0$ mA**

[PTO]

Output Waveform



if $-8V < V_i < 6V$,
$V_o = V_i$, $i_R = 0$

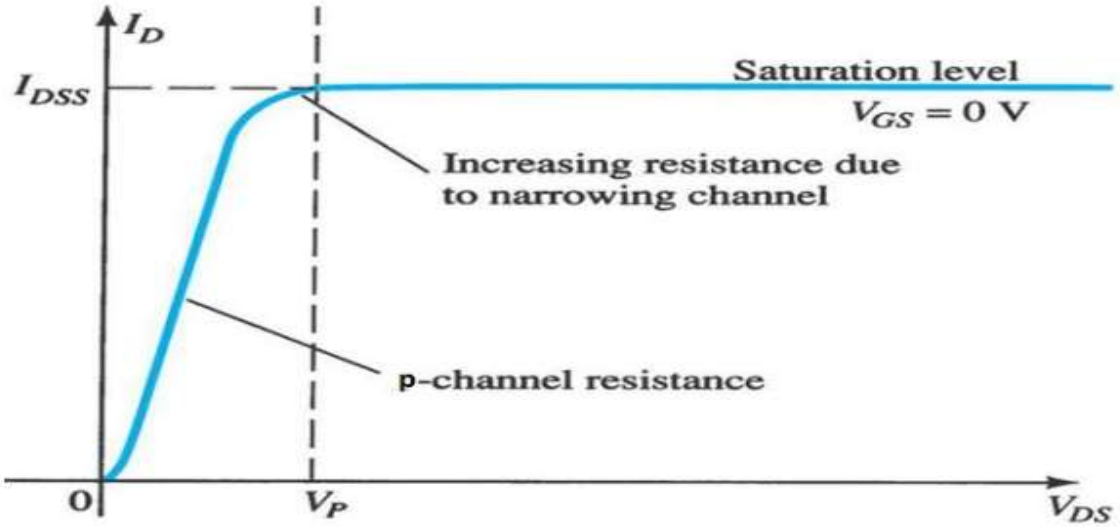
if $V_i > 6V$
$V_o = 6V$
$i_R = \frac{V_i - 6}{10}$ mA
Put $V_i = 10V$
$i_R|_{max} = \frac{10-6}{10} = 0.4mA$

if $V_i < -8V$
$V_o = -8V$
$i_R = \frac{V_i + 8}{10}$
Put $V_i = -10V$
$i_R|_{max} = \frac{-10+8}{10}$
$= -0.2mA$

UNIT-2

: Define Pinch-off voltage for JFET. (AKTU : 2022-23) (2 marks)

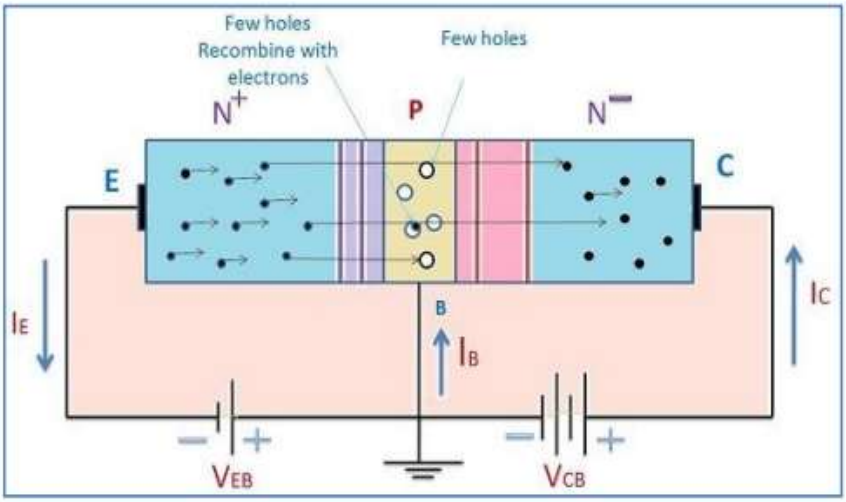
Sol. The minimum value of VDS at which current becomes saturated, is known as pinch-off voltage for V_{DS}.



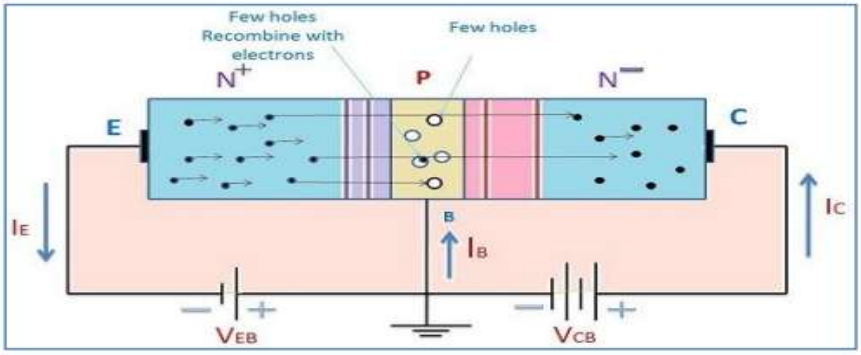
Ques 2 : Draw the circuit of NPN transistor in common base configuration and discuss its working. Draw input-output characteristic. (AKTU : 2022-23) (7 marks) & (AKTU : 2022-23) (10 marks)

Sol.

Working of NPN Transistor: The circuit diagram of the NPN transistor is shown in the figure below. The forward biased is applied across the emitter-base junction V_{BE}, and the reversed biased is applied across the collector-base junction V_{CB}. (Active Mode)



When the forward bias V_{BE} is applied across the emitter, the majority charge carriers (e^-)move towards the base. Some electrons recombine with holes and remaining enter into collector due to attraction force of reverse V_{CB}. The whole of the emitter current is entered into the base.



Thus, we can say that the emitter current is the sum of the collector or the base current.

$$I_E = I_B + I_C$$

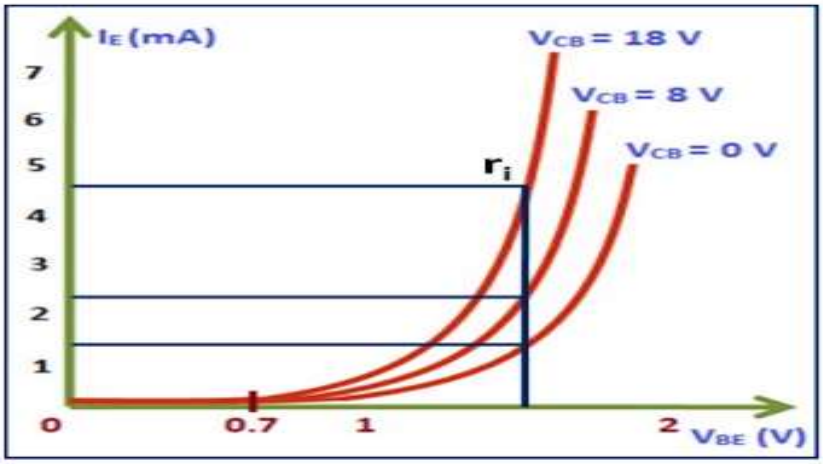
Input Characteristics in Common Base Configuration:

Input characteristics is drawn between Input Voltage V_{BE} and Input Current = I_E.

Output voltage $\mathbf{V_{CB}}$ is kept constant and the input voltage $\mathbf{V_{BE}}$ is increased from zero volts to different voltage levels. For each voltage level of the input voltage $\mathbf{(V_{BE})}$, the input current $\mathbf{(I_E)}$ is recorded on a paper or in any other form.

Input resistance $\mathbf{r_i}$ is the ratio of input voltage to input current.

$\mathbf{r_i = \Delta V_{BE} / \Delta I_E}$ **(For V_{CB} constant)**



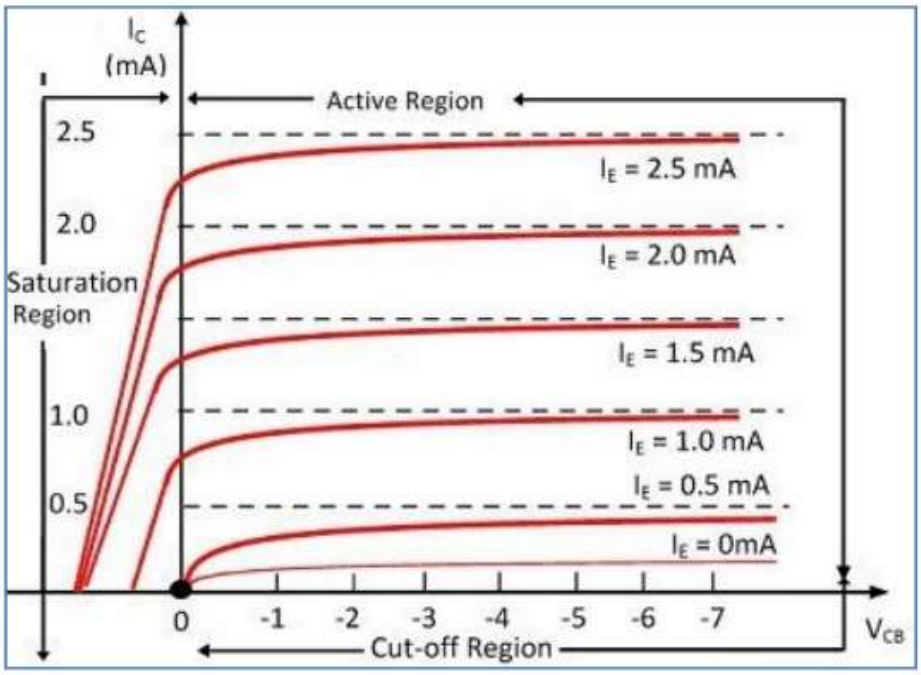
Output Characteristics in Common Base Configuration:

Output characteristics is drawn between Output Voltage = V_{CB} and Output Current = I_C.

Input current I_E is kept constant and the output voltage V_{CB} is increased from zero volts to different +ve and –ve voltage levels. For each voltage level V_{CB}, the output current (I_C) is recorded on a paper or in any other form.

Output resistance r_0 is the ratio of input voltage to input current.

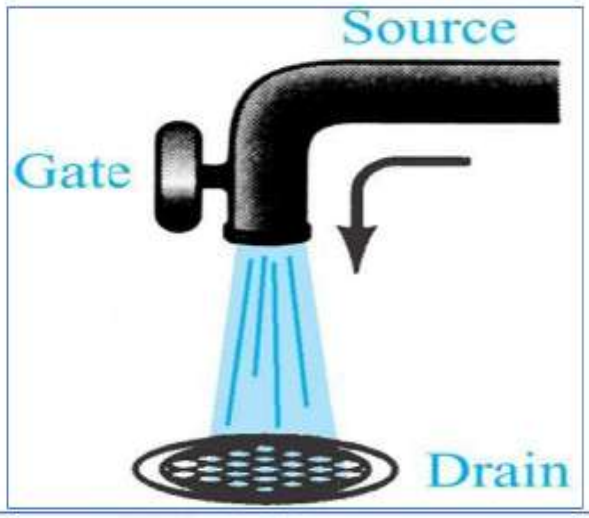
$r_0 = \Delta V_{CB} / \Delta I_C$ **(For I_E constant)**

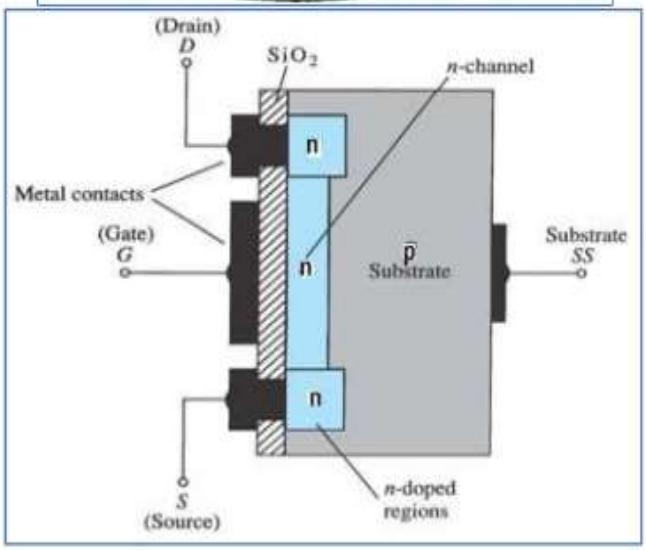


Ques 3: Explain working principle of Depletion type MOSFET (n-channel). Draw & Explain its characteristics. (AKTU : 2022-23) (7 marks)

Sol.

Unbiased n – channel Depletion MOSFET: In the absence of any applied voltage, MOSFET has a channel region between source and drain doped region. Neither drain to source voltage nor gate to source voltage is connected in MOSFET, which ensures no current flow in the circuit.



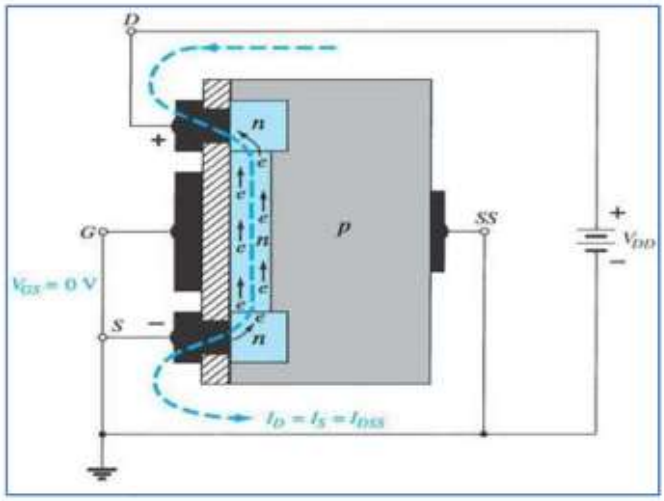


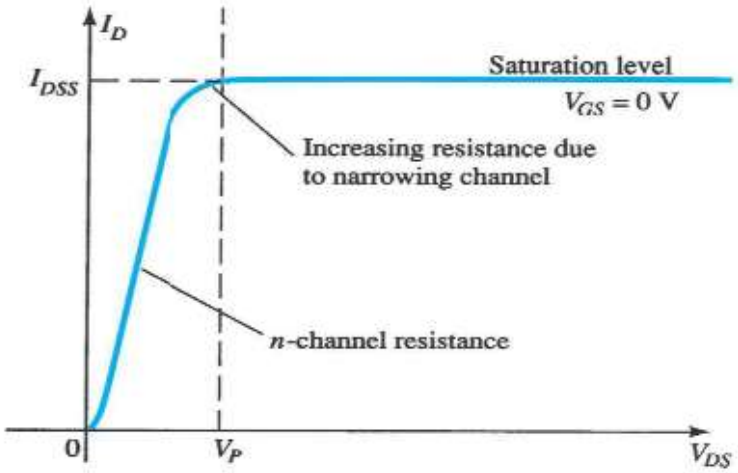
Operation in n – Channel Depletion MOSFET:

Case 1 When $V_{DS} \neq 0$ and $V_{GS} = 0$:

$V_{DS} > 0$ means V_{DS} is increased from 0 to a more positive voltage. Due to negative terminal of battery, electrons are generated from source region and electrons, due to positive terminal of battery, electrons are sink from drain region.

As we increase V_{DS} , number of electrons increases, hence current increases. But channel width is limited hence, on increasing V_{DS} , a condition arise when number of charge carries in the channel gets saturated, hence current gets saturated.





The minimum value of V_{DS} at which current becomes saturated, is known as pinch-off voltage for V_{DS} .
At $V_{GS} = 0$, Drain Current $I_D = I_{DSS}$

Case 2 When $V_{DS} \neq 0$ and $V_{GS} > 0$:

$V_{GS} > 0$ Gate terminal is excited with positive voltage. Hence it attracts electrons from p-substrate region towards n-channel. This enhance channel region.

Therefore maximum value of current in this case increases and becomes more than I_{DSS} .

This mode of operation is Enhancement Mode.

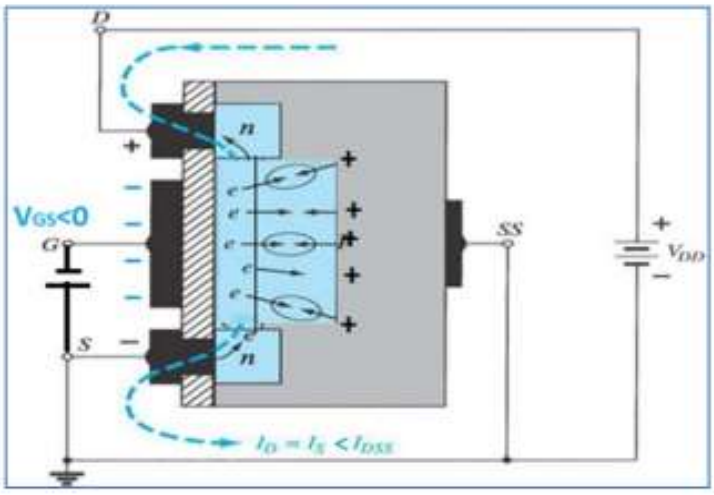
Hence for **$V_{DS} \neq 0$ and $V_{GS} > 0$,** **$I_D > I_{DSS}$.**

Case 3 When $V_{DS} \neq 0$ and $V_{GS} < 0$:

$V_{GS} < 0$ Gate terminal is excited with negative voltage. Hence it repels electrons from n-channel region towards p substrate where they recombine. This depletes channel region.

Therefore maximum value of current in this case decreases and becomes less than I_{DSS} .

This mode of operation is Depletion Mode. **$I_D < I_{DSS}$.**



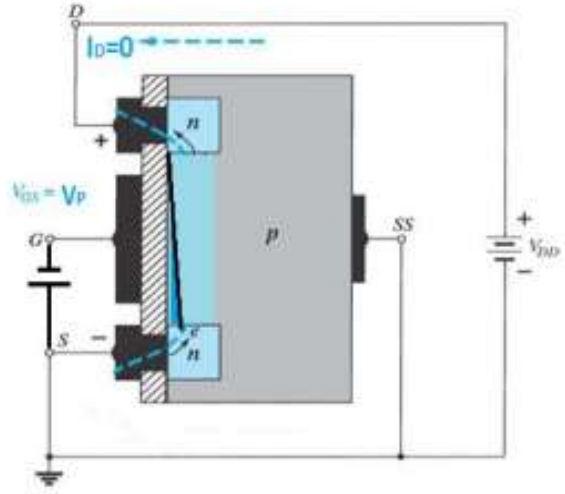
Case 4 When $V_{DS} \neq 0$ and $V_{GS} = V_P$:

$V_{GS} < 0$ means gate terminal I negative. As we increases V_{GS} in negative direction, a condition arise when number of electrons are insufficient to carry out conduction, means channel is completely depleted. This condition is known as Pinch-off condition . The drain current in this case becomes 0.

The value of V_{GS} at which I_D becomes 0, is pinch-off voltage.

Hence, $V_P = V_{GS} \mid_{ID=0}$

Hence for **$V_{DS} \neq 0$ and $V_{GS} = V_P$, $I_D = 0$.**



The current I_D varies with V_{GS} as the following current equation, which is known as Shockley Equation.

Hence, according to Shockley Equation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

When $V_{GS} = 0$, $I_D = I_{DSS}$

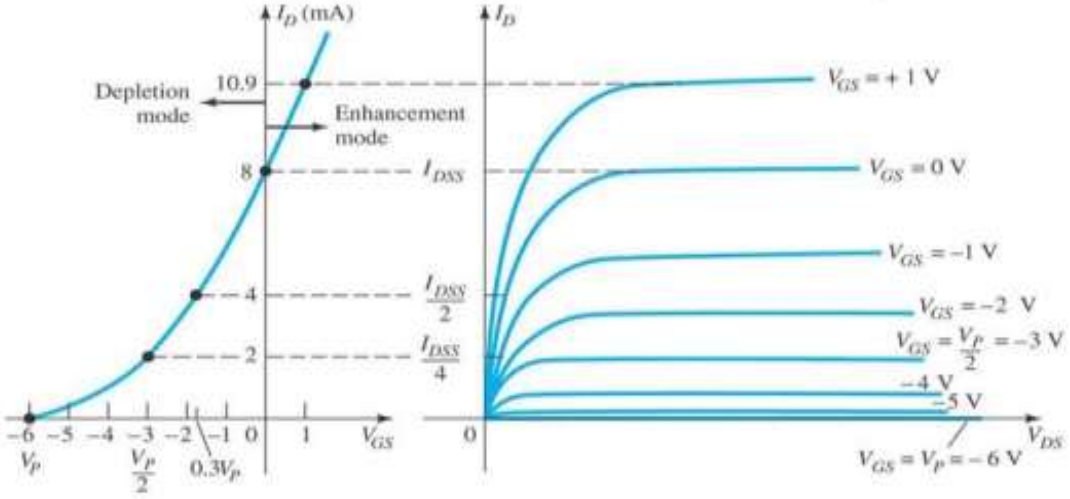
When $V_{GS} > 0$, $I_D > I_{DSS}$

When $V_{GS} < 0$, $I_D < I_{DSS}$

(Moderate Current following Shockley Equation)

When $V_{GS} = V_P$, $I_D = 0$ (Minimum Current)

Transfer Characteristics and Output or Drain Characteristics Curve of n – Channel Depletion MOSFET:



The plot between V_{DS} and I_D is known as output characteristics.

As we increase V_{DS}, output current increases up to a certain value and gets saturated for different V_{GS} voltage level.

Plot between V_{GS} and I_D is known as Transfer Characteristics Curve. This is quadratic in nature due to its current equation.

As we increase V_{GS}, output current decreases following Shockley Equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

When $V_{GS} = 0$, $I_D = I_{DSS}$

When $V_{GS} = V_P$, $I_D = 0$

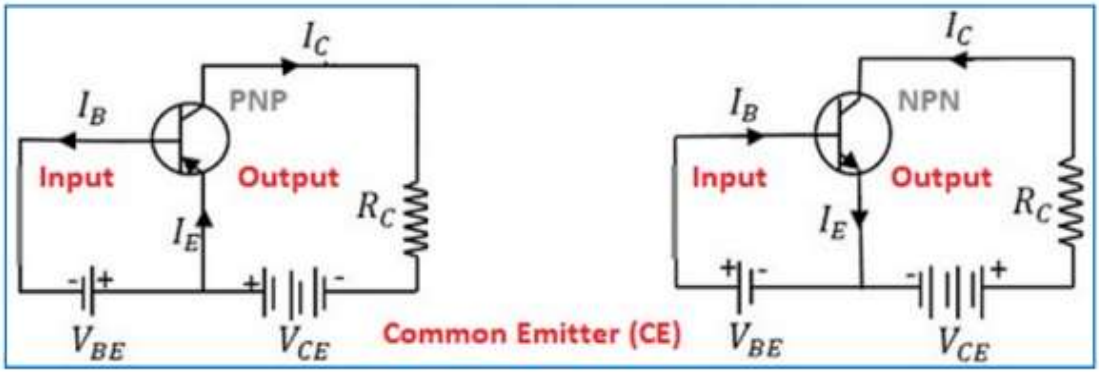
Ques 4 : Why FET is called as voltage controlled devices? (AKTU : 2022-23) (2 marks)

Sol. Since in an FET the value of the current depends upon the value of the voltage applied at the gate and drain so it is known as voltage controlled device. For example: In a MOSFET, the current from drain to source depends upon the width of the depletion layer which in turn depends upon the voltage applied on the gate so that is the reason.

Ques 5 : Draw and explain the working of N-P-N transistor in common emitter configuration with its suitable characteristics graph. (AKTU : 2022-23) (7 marks) & (AKTU : 2021-22) (10marks)

Sol.

Common Emitter Configuration: In the case of the **Common Emitter (CE) configuration**, the emitter terminal is common between the input and the output side.



Since base region is thin and collector region is thick, Base-Emitter becomes input port while Collector-Emitter becomes output port.

Hence, Input Voltage = $\mathbf{V_{BE}}$ Input Current = $\mathbf{I_B}$

Output Voltage = $\mathbf{V_{CE}}$ Output Current = $\mathbf{I_C}$

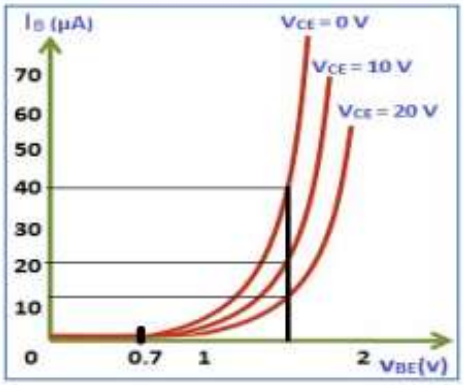
Input Characteristics in Common Emitter Configuration:

Input characteristics is drawn between Input Voltage V_{BE} and Input Current = I_B.

Output voltage $\mathbf{V_{CE}}$ is kept constant and the input voltage $\mathbf{V_{BE}}$ is increased from zero volts to different voltage levels. For each voltage level of the input voltage **(V_{BE})**, the input current **(I_B)** is recorded on a paper or in any other form.

Input resistance $\mathbf{r_i}$ is the ratio of input voltage to input current.

$\mathbf{r_i = \Delta V_{BE} / \Delta I_B}$ **(For V_{CE} constant)**



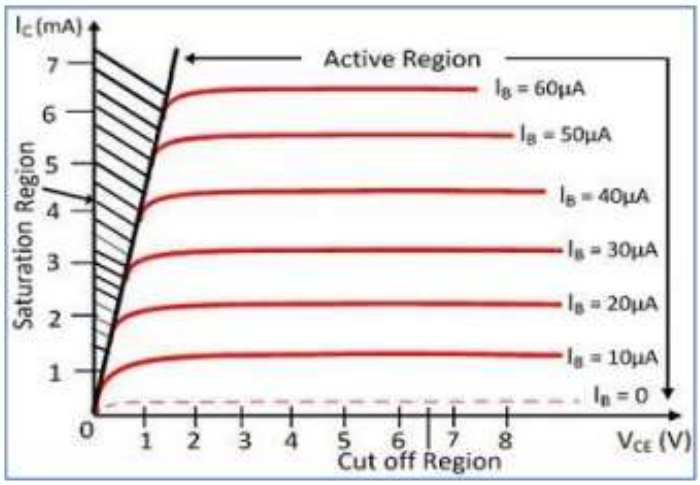
Output Characteristics in Common Emitter Configuration:

Output characteristics is drawn between Output Voltage = V_{CE} and Output Current = I_C.

Input current $\mathbf{I_B}$ is kept constant and the output voltage $\mathbf{V_{CE}}$ is increased from zero volts to different +ve and –ve voltage levels. For each voltage level $\mathbf{V_{CE}}$, the output current $\mathbf{(I_C)}$ is recorded on a paper or in any other form.

Output resistance $\mathbf{r_0}$ is the ratio of input voltage to input current.

$\mathbf{r_0 = \Delta V_{CE} / \Delta I_C}$ **(For I_B constant)**



Common Emitter Configuration:

Input characteristics is drawn between Input Voltage V_{BE} and Input Current = I_B, however Output characteristics is drawn between Output Voltage = V_{CE} and Output Current = I_C.

Current Gain or Current Amplification Factor (β): It is defined as the ratio of output current I_C to input current I_B in CE configuration. $\mathbf{\beta_{dc} = \alpha = I_C / I_B}$ **(In static conditions)**

And $\beta_{ac} = \Delta I_C / \Delta I_B$ **(In dynamic conditions)**

Leakage Current: In input is not connected in the circuit, a reverse current flows in the reverse bias Collector-Emitter junction denoted by I_{CEO} (Collector to Emitter Leakage Current).

So majority current $I_C = \beta I_B$ and minority current $I_C = I_{CEO}$

Hence output current $I_C = \beta I_B + I_{CEO}$

Ques 6 : Differentiate BJT and JFET. (AKTU:2021-22) (2 marks)

Sol.

BJT	FET
1. Current controlled devices	1. Voltage controlled devices
2. Lower impedance	2. Higher input impedance
3. Higher sensitive	3. Less sensitive to temp. variations
4. Bipolar device	4. Unipolar device
5. Bigger IC	5. Smaller/ Easily Integrated Chips
6. Terminals: Base Emitter, Collector	6. Terminals: Gate, Source, Drain

Ques 7: Define Transconductance of JFET. (AKTU:2021-22) (2 marks)

Sol.

Trans-conductance in JFET :

It is defined as the ratio of change in drain current to change in gate to source voltage.

$$g_m = \partial I_D / \partial V_{GS}$$

Derivation:

We know that $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Differentiating w.r.t. V_{GS}

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right] = -\frac{2\,I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Ques 8 : Define α and β with respect to BJT and also derive the relationship between them. (AKTU : 2021-22) (5 marks)

Sol.

Current Gain or Current Amplification Factor (α): It is defined as the ratio of output current I_C to input current I_E in CB configuration. $\alpha_{dc} = \alpha = I_C / I_E$ **(In static conditions)**

And $\alpha_{ac} = \Delta I_C / \Delta I_E$ **(In dynamic conditions)**

Current Gain or Current Amplification Factor (β): It is defined as the ratio of output current I_C to input current I_B in CE configuration. $\beta_{dc} = \alpha = I_C / I_B$ **(In static conditions)**

Relation Between α and β:

We know that $\alpha = I_C / I_E$ and $\beta = I_C / I_B$ and $I_E = I_B + I_C$

Divide this equation by I_C in both the sides,

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad or, \quad \frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\alpha = \frac{\beta}{1+\beta}$$

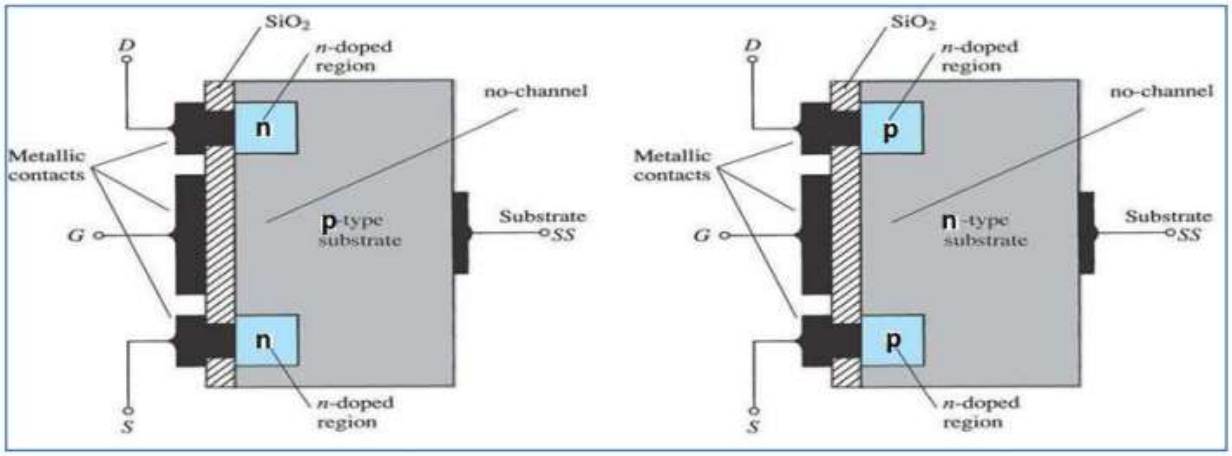
$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad or, \quad \frac{1}{\beta} = \frac{1}{\alpha} - 1 \quad or, \quad \frac{1}{\beta} = \frac{1-\alpha}{\alpha}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

Ques 9: Explain the working of enhancement type MOSFET along with their transfer characteristics. (AKTU : 2021-22) (10 marks)

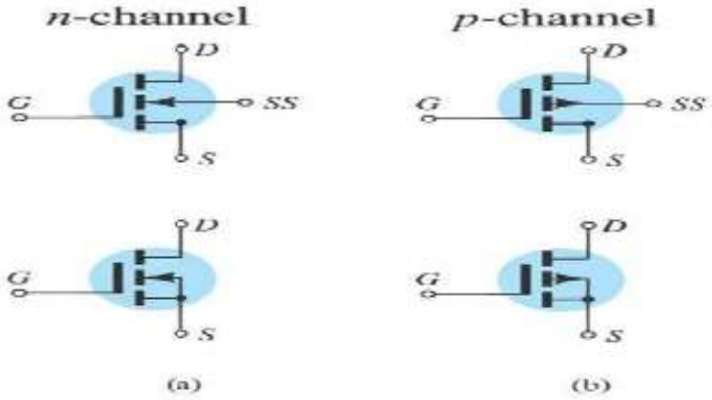
Sol.

Enhancement Type MOSFET: Construction: The Drain (D) and Source (S) connect to the doped regions. Between these doped regions, channel is present in channel region. Channel region is connected to the Gate (G) via a thin insulating layer of SiO2. There is no direct electrical connection between the gate terminal and the channel of a MOSFET. This ensures very high input impedance in MOSFET. The doped material lies on a doped substrate of opposite material.



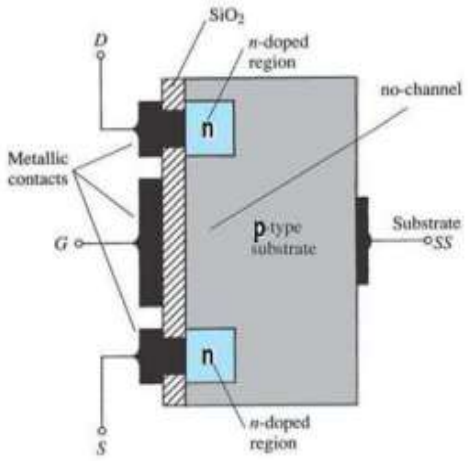
N-Channel E MOS **P-Channel E MOS**

Enhancement Type MOSFET: Symbols:



n – Channel Enhancement MOSFET: (1) unbiased: Neither drain to source voltage nor gate to source voltage is connected in MOSFET, which ensures no current flow in the circuit.

(2) When $V_{DS} \neq 0$ and $V_{GS} = 0$: Since channel is not present, so there is no any path for current conduction. Hence no current flow in the circuit.



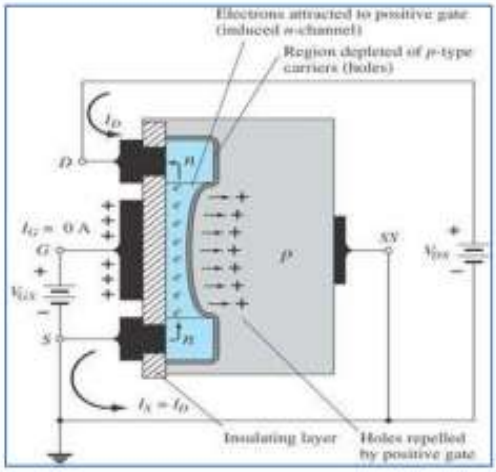
Operation in n – Channel Enhancement MOSFET:

Case 1 When $V_{DS} \neq 0$ and $V_{GS} > 0$:

$V_{DS} > 0$ means V_{DS} is increased from 0 to a more positive voltage. Due to negative terminal of battery, electrons are generated from source region and electrons, due to positive terminal of battery, electrons are sink from drain region.

When $V_{GS} > 0$,

As we increase V_{GS} , electrons are attracted towards the channel region. A condition arise when, number of electrons are sufficient to form channel. Hence, current starts flowing. The value of V_{GS} at which MOSFET starts conducting is threshold voltage. It is denoted by V_t .



As we increase V_{DS} , current increases up to a certain value and then saturates.

The current I_D varies with V_{GS} as the following current equation,

$$I_D = k(V_{GS} - V_t)^2$$

Hence, according to the Equation,

When $V_{GS} = 0$, $I_D = 0$

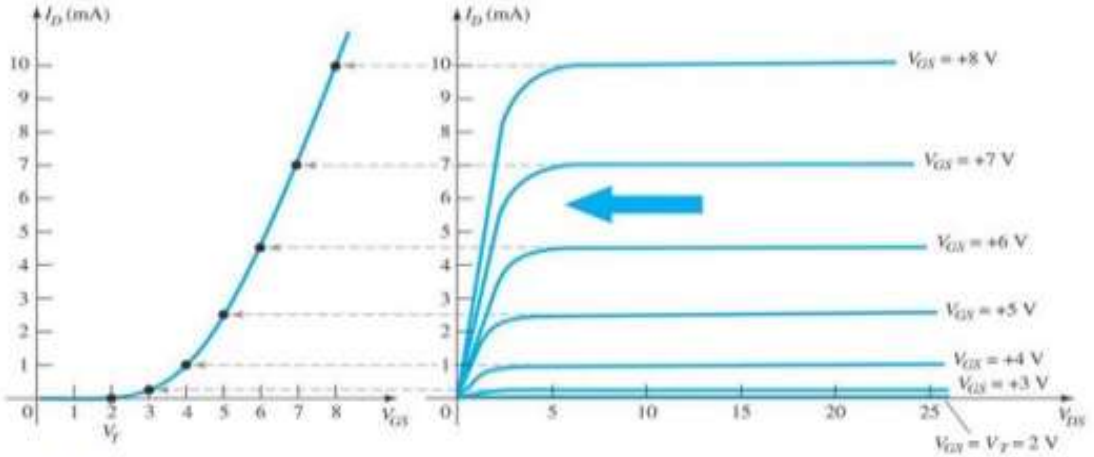
When $V_{GS} < 0$, $I_D = 0$

When $V_{GS} > 0$, but $V_{GS} < V_t$, $I_D = 0$

When $V_{GS} > 0$, but $V_{GS} > V_t$, $I_D \neq 0$

Where V_t is threshold voltage of n channel E MOSFET.

Transfer Characteristics and Output or Drain Characteristics Curve of n – Channel Enhancement MOSFET :



The plot between V_{DS} and I_D is known as output characteristics.

As we increase V_{DS} , output current increases up to a certain value and gets saturated for different V_{GS} voltage level.

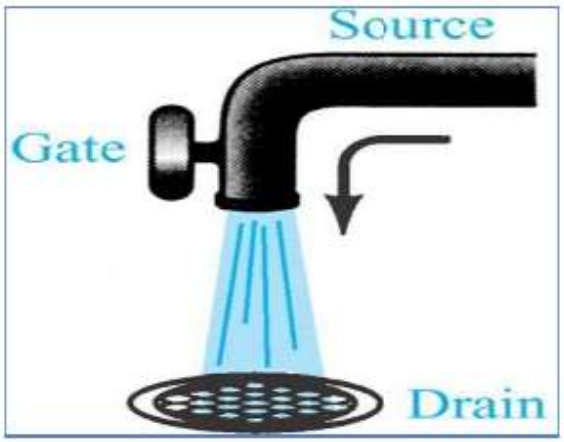
Plot between V_{GS} and I_D is known as Transfer Characteristics Curve. This is quadratic in nature due to its current equation. As we increase V_{GS} , output current increases following Equation.

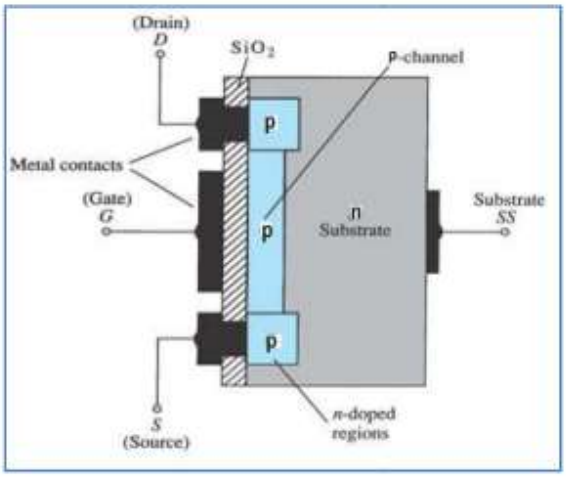
$$I_D = k(V_{GS} - V_t)^2$$

Ques 10 : Describe the construction and working of P-Channel Depletion MOSFET, with characteristic graph. Also Justify that it is a voltage controlled device. (AKTU : 2021-22) (10 marks)

Sol.

Unbiased p – channel Depletion MOSFET: In the absence of any applied voltage, MOSFET has a channel region between source and drain doped region. Neither drain to source voltage nor gate to source voltage is connected in MOSFET, which ensures no current flow in the circuit.



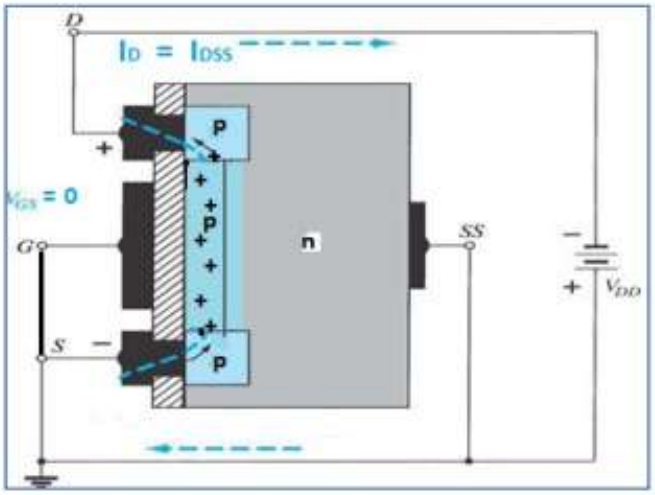


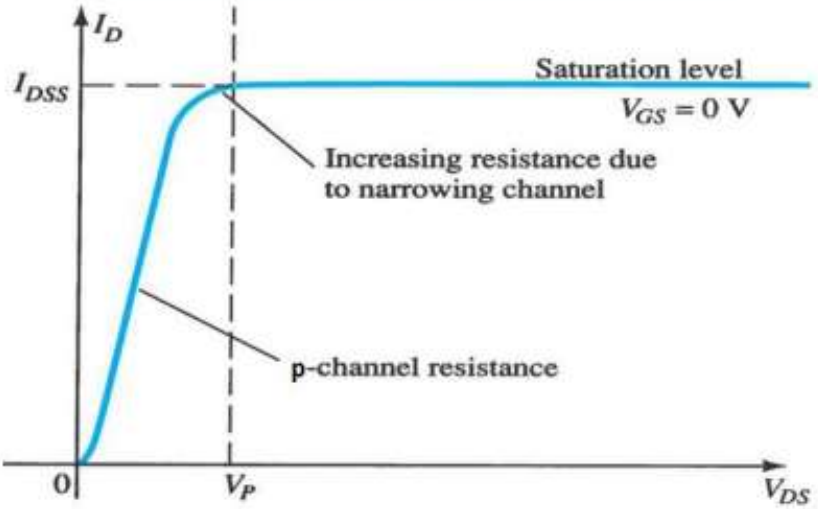
Operation in p – Channel Depletion MOSFET:

Case 1 When $V_{DS} \neq 0$ and $V_{GS} = 0$:

$V_{DS} > 0$ means V_{DS} is increased from 0 to a more positive voltage. Due to negative terminal of battery, holes are generated from source region and due to positive terminal of battery, holes are sink from drain region.

As we increase V_{DS} , number of holes increases, hence current increases. But channel width is limited hence, on increasing V_{DS} , a condition arise when number of charge carries in the channel gets saturated, hence current gets saturated.





The minimum value of V_{DS} at which current becomes saturated, is known as pinch-off voltage for V_{DS} .
At $V_{GS} = 0$, Drain Current $I_D = I_{DSS}$

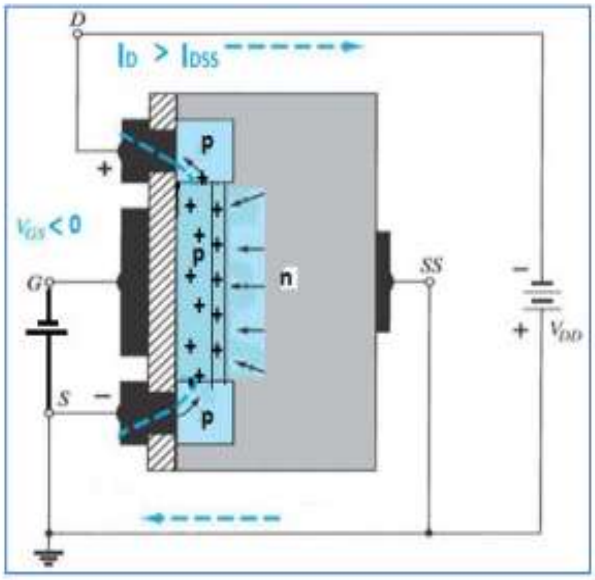
Case 2 When $V_{DS} \neq 0$ and $V_{GS} < 0$:

$V_{GS} < 0$ Gate terminal is excited with negative voltage. Hence it attracts holes from n-substrate region towards p-channel. This enhance channel region.

Therefore maximum value of current in this case increases and becomes more than I_{DSS} .

This mode of operation is Enhancement Mode.

Hence for **$V_{DS} \neq 0$ and $V_{GS} < 0$, $I_D > I_{DSS}$.**



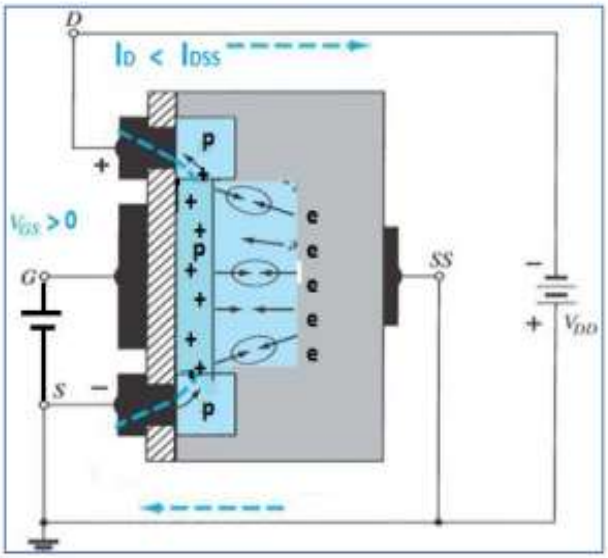
Case 3 When $V_{DS} \neq 0$ and $V_{GS} > 0$:

$V_{GS} > 0$ Gate terminal is excited with positive voltage. Hence it repels holes from p-channel region towards n substrate where they recombine. This depletes channel region.

Therefore maximum value of current in this case decreases and becomes less than I_{DSS} .

This mode of operation is Depletion Mode.

Hence for **$V_{DS} \neq 0$ and $V_{GS} > 0$,** **$I_D < I_{DSS}$.**



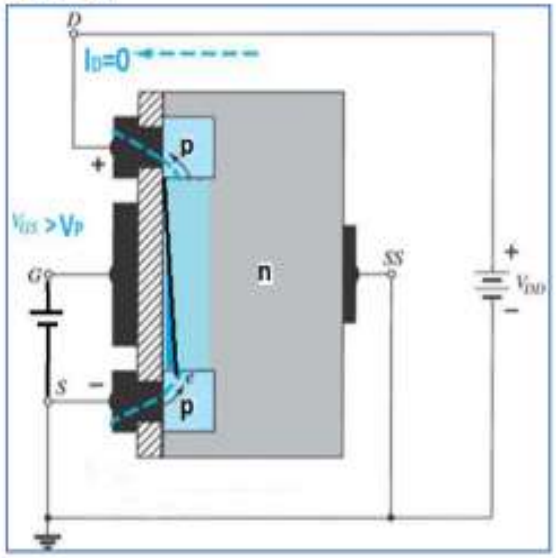
Case 4 When $V_{DS} \neq 0$ and $V_{GS} = V_P$:

$V_{GS} < 0$ means gate terminal is positive. As we increases V_{GS} in positive direction, a condition arise when number of holes are insufficient to carry out conduction, means channel is completely depleted. This condition is known as Pinch-off condition . The drain current in this case becomes 0.

The value of V_{GS} at which I_D becomes 0, is pinch-off voltage.

Hence, $V_P = V_{GS} \mid_{ID=0}$

Hence for $V_{DS} \neq 0$ **and** $V_{GS} = V_P$, $I_D = 0$.



The current I_D varies with V_{GS} as the following current equation, which is known as Shockley Equation.

Hence, according to Shockley Equation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

When $V_{GS} = 0$, $I_D = I_{DSS}$

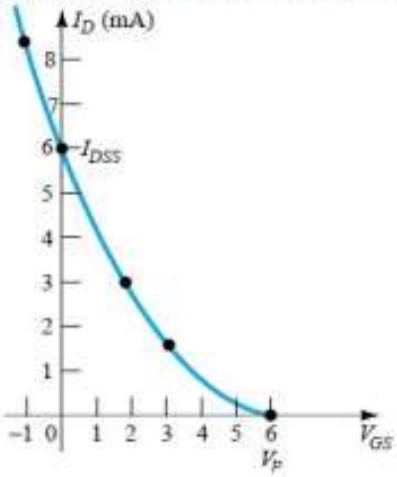
When $V_{GS} < 0$, $I_D > I_{DSS}$

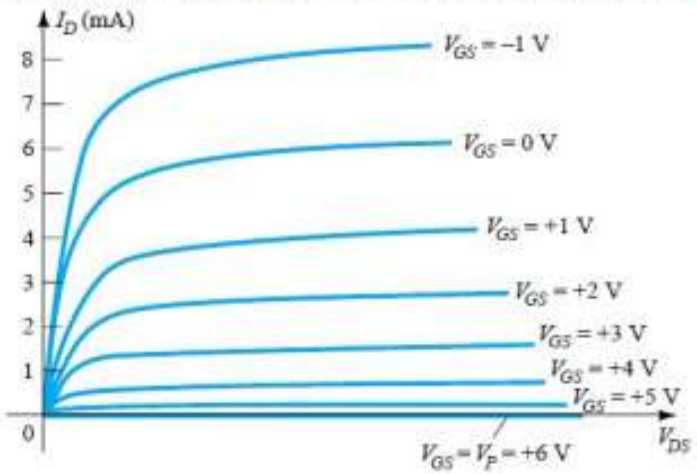
When $V_{GS} > 0$, $I_D < I_{DSS}$

(Moderate Current following Shockley Equation)

When $V_{GS} = V_P$, $I_D = 0$ (Minimum Current)

Transfer Characteristics and Output or Drain Characteristics Curve of p – Channel Depletion MOSFET :





Numerical

Numerical: Calculate current gain in CB configuration if collector and emitter currents are 5.10 mA and 5.18 mA. Hence calculate current gain of same BJT in CE and CC configurations.

Solution: Given that, $I_C = 5.10$ mA and $I_E = 5.18$ mA

we know that $\alpha = I_C / I_E = 5.10 / 5.18 = 0.985$

or, **$\alpha = 0.985$**

We know that $\beta = \alpha / (1 - \alpha) = 0.985 / (1 - 0.985) = 0.985 / 0.015$

Or, **$\beta = 65.667$**

We know that $\gamma = 1 + \beta = 1 + 65.667$

Or, **$\gamma = 66.667$**

Numerical: If β of a transistor is 100 and emitter current is 10 mA with I_{CBO} = 10 µA. Calculate base and collector currents.

Solution: given that, $\beta = 100$, $I_E = 5.18$ mA, $I_{CBO} = 10$ µA

We know that Collector current $I_C = \alpha I_E + I_{CBO}$

So first we find, $\alpha = \beta / (1 + \beta) = 100 / 101 = 0.99$

Hence, **$\alpha = 0.99$**

Hence, Collector current $I_C = \alpha I_E + I_{CBO}$

$= 0.99 \times 10$ mA $+ 0.010$ mA $= 9.91$ mA

Hence, **$I_C = 9.91$ mA**

Hence, Base current $I_B = I_E - I_C = 10 - 9.91$ mA $= 0.090$ mA

Hence, **$I_B = 0.090$ mA $= 90$ µA**

Numerical: In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 µA. Find the total collector current, Base current, β and I_{CEO}. Given that α = 0.92.

Solution: given that, $\alpha = 0.92$, $I_E = 1$ mA, $I_{CBO} = 50$ µA

We know that Collector current **$I_C = \alpha I_E + I_{CBO}$**

Hence, $I_C = 0.92 \times 1 + 0.050 = 0.97$ mA or, **$I_C = 0.97$mA**

Now Base Current **$I_B = I_E - I_C$**

Hence, $I_B = 1 - 0.97 = 0.03$ mA $= 30$ µA or, **$I_B = 30$ µA**

Now, **$\beta = \alpha / (1 - \alpha)$** $= 0.92 / (1 - 0.92)$

Hence, $\beta = 0.92 / 0.08 = 11.5$ or, **$\beta = 11.5$**

Now, **$I_{CEO} = (1 + \beta) I_{CBO}$**

Hence, $I_{CEO} = (1 + 11.5) \times 50 = 625$ µA or, **$I_{CEO} = 625$ µA**

Numerical: In a JFET, I_{DSS} = 8mA, V_{GS} = –6V and V_P = –8V, Calculate, I_D , g_m and g_{m0} . Also calculate r_d if r_0 = 23Ω.

Solution: We know that

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 8\times\left(1-\frac{6}{8}\right)^2 = 0.5\ mA$$

$$g_m = \left|\frac{2\,I_{DSS}}{V_P}\right|\left(1-\frac{V_{GS}}{V_P}\right) = \frac{2\times 8}{8}\times\left(1-\frac{6}{8}\right) = 0.5\ \Omega^{-1}$$

$g_{m0} = | 2I_{DSS} / V_P | = 2 \times 8 / 8 = 2\ \Omega^{-1}$

We know that

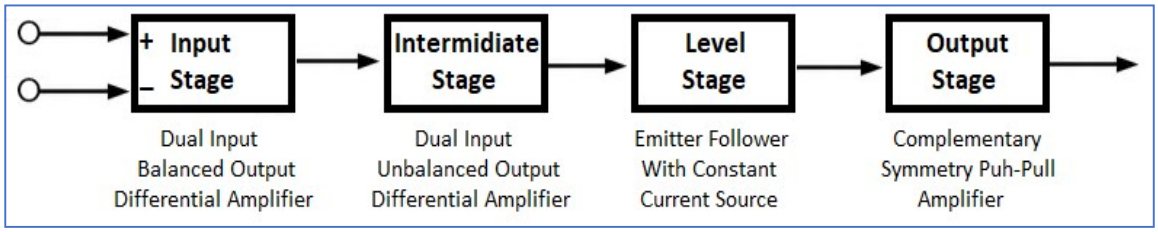
$$r_d = \frac{r_0}{\left(1-\frac{V_{GS}}{V_P}\right)^2} = \frac{23}{\left(1-\frac{6}{8}\right)^2}$$

Answer: I_D = 0.5 mA, g_m = 0.5 Ω^{-1} , g_{m0} = 2 Ω^{-1} , r_d = 368 Ω

UNIT-3

OPERATIONAL AMPLIFIER

Q1: Draw and explain Block Diagram of Op-amp. (AKTU :2020-21)(10 MARKS)
Block Diagram of Operational Amplifier:



OPAMP is basically a differential amp. It will amplify the voltage which is differentially present between its input terminals.

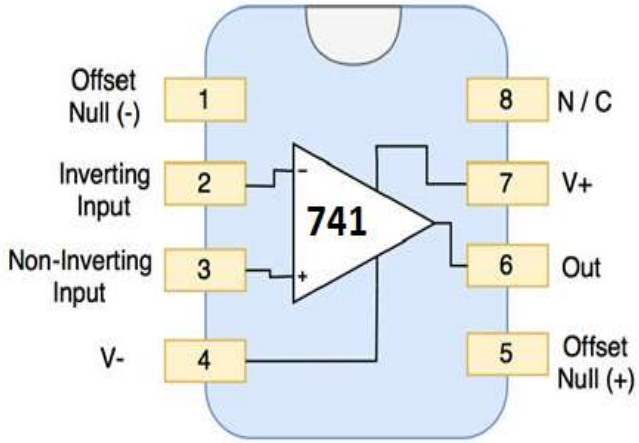
Input or Gain stage: The input stage is a dual input, balanced output differential amp. The 2 inputs are inverting and non- inverting input terminals. This stage provides most of the voltage gain of the OP-AMP and decides the value of input resistance R_i.

Intermediate stage: This is usually another differential amp. The input stage drives the stage. The stage is a dual input unbalanced o/p differentiated amp.

Level- shifting stage: Due to direct coupling used between the 1st 2 stages, the i/p of level shifting stage is an amplified signal with some non – zero dc level. Level shifting stage is used to bring dc level to zero volts with respect to gnd.

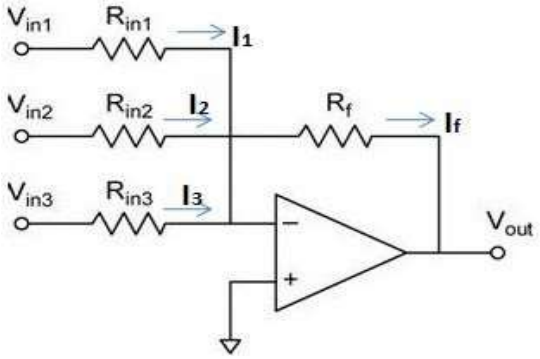
Output stage: This stage is normally a complementary o/p stage. It increases the magnitude of voltage and raises the current supplying capability of OP-AMP. It also ensures that the o/p resistance of OPAMP is low.

Q2: Draw and explain IC Diagram of Op-amp 741.
IC Diagram of IC 741



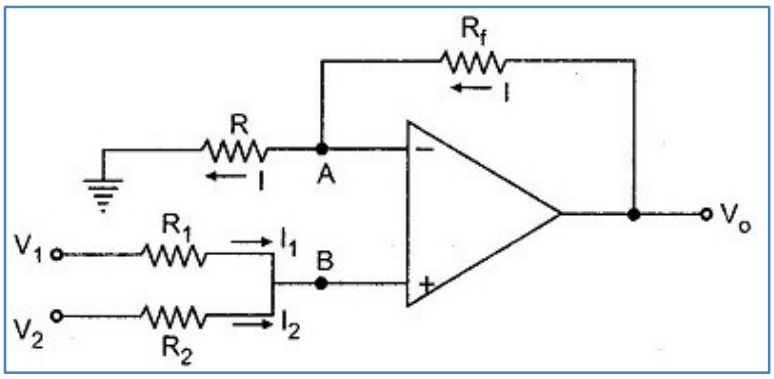
Pin4 & Pin7 (Power Supply): Pin7 is the positive voltage supply terminal and Pin4 is the negative voltage supply terminal. The 741 IC draws in power for its operation from these pins. The voltage between these two pins can be anywhere between 5V and 18V.
Pin6 (Output): This is the output pin of IC 741. The voltage at this pin depends on the signals at the input pins and the feedback mechanism used.
Pin2 & Pin3 (Input): These are input pins for the IC. Pin2 is the inverting input and Pin3 is the non-inverting input. If the voltage at Pin2 is greater than the voltage at Pin3, i.e., the voltage at inverting input is higher, the output signal stays low. Similarly, if the voltage at Pin3 is greater than the voltage at Pin2, i.e., the voltage at non-inverting input is high, the output goes high.
Pin1 & Pin5 (Offset Null): Because of high gain provided by 741 Op-Amp, even slight differences in voltages at the inverting and non-inverting inputs, caused due to irregularities in manufacturing process or external disturbances, can influence the output. To nullify this effect, an offset voltage can be applied at pin1 and pin5, and is usually done using a potentiometer.
Pin8 (N/C): This pin is not connected to any circuit inside 741 IC. It's just a dummy lead used to fill the void space in standard 8 pin packages. (N/C – Not Connected)

Q3: Draw following circuits using Op-amp and derive its output voltage.
(a) Inverting Summing Amplifier, (b) Non-Inverting Summing Amplifier
Summing Amplifier: (a) Inverting Summing Amplifier: It is defined an electronic circuit which provide addition of all the inputs applied at inverting terminal.



Voltages, $V_A = V_B = 0$ (Ground)
Applying KCL at node A,
Currents, $I_1 + I_2 + I_3 = I_f$
Or, $(V_1 – V_A)/R_1 + (V_2 – V_A)/R_2 + (V_3 – V_A)/R_3 = (V_A – V_0)/ R_f$
but $V_A = 0$ Hence, $V_1/R_1 + (V_2/R_2 + (V_3/R_3 = – V_0/ R_f$
Hence, $\mathbf{V_0 = – R_f V_1 / R_1 – R_f V_2 / R_2 – R_f V_3 / R_3}$
If $R_1 = R_2 = R_3 = R_f$ then Or,
$\mathbf{V_0 = – V_1 – V_2 – V_3}$
$\mathbf{V_0 = – (V_1 + V_2 + V_3)}$

Summing Amplifier: (b) Non-Inverting Summing Amplifier: It is defined a an electronic circuit which provide addition of all the inputs applied at non inverting terminal. (in diagram)



Now at node B, $I_1 + I_2 = 0$

Or, $(V_1 - V_B) / R_1 + (V_2 - V_B) / R_2 = 0$ Or, $V_B = (R_1 V_2 + R_2 V_1)/(R_1 + R_2)$

Due to virtual connection concept,

Voltages, $V_A = V_B = (R_1 V_2 + R_2 V_1)/(R_1 + R_2)$

Applying KCL at node A, Currents, $I = I_f$

Or, $(0 - V_A)/ R_{in} = (V_A - V_0)/ R_f$ or,

$-V_A / R_{in} = V_A / R_f - V_0 / R_f$ Or,

$V_0 / R_f = V_A / R_f + V_A / R_{in}$ or,

$V_0 = (1 + R_f / R_{in}) V_A$

Now **$V_0 = (1 + R_f / R_{in}) V_A$**

Putting value of $V_A = (R_1 V_2 + R_2 V_1)/(R_1 + R_2)$

Voltage, $V_0 = (1 + R_f / R_{in}) (R_1 V_2 + R_2 V_1)/(R_1 + R_2)$

Let $R_1 = R_2 = R_f = R_{in}$

$V_0 = (1 + 1) (V_2 + V_1)/ 2$

Or, **$V_0 = V_2 + V_1$**

Q4: List Characteristics and their ideal values of an op-amp. (AKTU :2020-21)(10 MARKS)

Op-amp Characteristics:

Parameters	**Ideal Values**	**Practical Values**
Bandwidth	∞	Approximately all bands
Input Current	0	< 0.1 μA
Input Impedance	∞	> 10^7 Ω
Output Impedance	0	< 100 Ω
Open Loop Voltage Gain or Differential Gain (A_0 or A_d)	∞	> 10^6
Common Mode Gain	0	< 5

Common Mode Rejection Ratio (CMRR)	∞	$> 10^5$
Slew Rate	∞	> 2 V/μs
Input/output Offset Voltage	0	< 50 mV
Input Offset or Bias Current	0	< 50 nA

Q5: Define and explain following terms:

(a) Slew Rate, (b) Input Bias Current, (c) Input Impedance, (d) Common Mode Rejection Ratio

(a) Slew Rate: It is defined as the response rate or response speed of the op-amp. Let change in output is dV_0 against the input applied to the op-amp after dt time.

Then Slew Rate (SR) = dV_0 / dt

Ideally dt = 0 μs hence, SR = $dV_0 / 0 = \infty$

(b) Input Bias Current: It is defined as the minimum input current required to bias an input so that input voltage can be responded at output terminal.

Ideally it is $I_{bias} = 0$ nA.

(c) Input Impedance: It is defined as the ratio of input voltage to input current in the op-amp.

$R_i = V_{id} / I_i$

Ideally $I_i = 0$ hence $R_i = V_{id} / 0 = \infty$

(d) Common Mode Rejection Ratio: It is defined as the ration of differential gain to common mode gain of Op-amp. **$CMRR = A_d / A_{CM}$**

We know that Output Voltage $V_0 = A_d V_d + A_{CM} V_{CM}$

Where, A_d = Differential Gain, and A_{CM} = Common Mode Gain

Ideally $A_d = \infty$, and $A_{CM} = 0$ Hence, $CMRR = A_d / 0 = \infty$

Calculation of CMRR in dB

For practical Op-amp, $CMRR = A_d / A_{CM}$

Taking log in both the sides, $\log (CMRR) = \log (A_d / A_{CM})$

Or, $\log (CMRR) = \log A_d - \log A_{CM}$

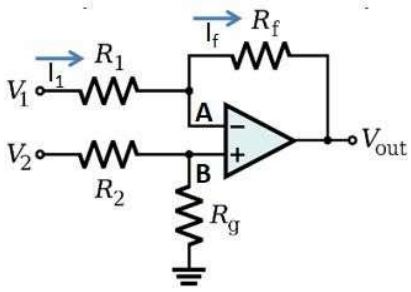
Multiply by 10 in both the sides,

$10\log (CMRR) = 10\log A_d - 10\log A_{CM}$

Or, **$CMRR\ (dB) = A_d\ (dB) - A_{CM}\ (dB)$**

Q6: Draw Difference Amplifier using Op-amp and derive its output voltage.

Difference Amplifier: It is defined as an electronic circuit which provides subtraction of inverting input from non-inverting input applied to the Op-amp.



Now at node B, Using potential division rule, Or,

$V_B = V_2 R_g / (R_g + R_2)$

Due to virtual connection concept, Voltages,

$V_A = V_B = V_2 R_g / (R_g + R_2)$

Applying KCL at node A,

Currents, $I = I_f$

Or, $(V_1 - V_A)/ R_1 = (V_A - V_0)/ R_f$

or, $V_1 / R_1 - V_A / R_1 = V_A / R_f - V_0 / R_f$

Or, $V_0 / R_f = V_A / R_f + V_A / R_1 - V_1 / R_1$

or, $\mathbf{V_0 = (1 + R_f / R_1) V_A - R_f V_1 / R_1}$

But $V_A = V_2 R_g / (R_g + R_2)$

Hence, $V_0 = (1 + R_f / R_1) V_A - R_f V_1 / R_1$

Or, $\mathbf{V_0 = (1 + R_f / R_1) V_2 R_g / (R_g + R_2) - R_f V_1 / R_1}$

Let $R_1 = R_2 = R_f = R_g = R$

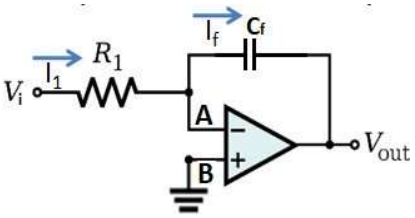
Then, $\mathbf{V_0 = (1 + 1) V_2 / 2 - V_1}$

Or, $\mathbf{V_0 = V_2 - V_1}$

Q7: Draw following circuits using Op-amp and derive its output voltage.(AKTU:2021-22)(10 MARKS)

(a) Integrator, (b) Differentiator

Integrator Amplifier: It is defined as an electronic circuit which provides integration of input applied to the Op-amp in output of the op-amp.



Due to virtual connection concept, $V_A = V_B = 0$ (Ground)

Applying KCL at node A, $I_1 = I_f$

$(V_i - V_A)/ R_1 = C_f \, d(V_A - V_0)/dt$

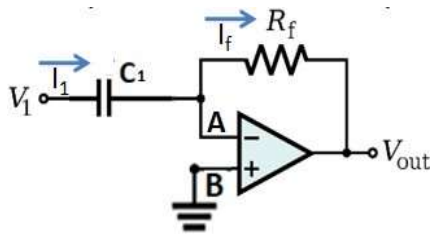
But $V_A = 0$

$(V_i - 0)/ R_1 = C_f \, d(0 - V_0)/dt$

$$dV_0 = -\frac{1}{R_1 C_f} V_i dt$$

$$\boxed{V_0 = -\frac{1}{R_1 C_f}\int V_i dt + K}$$

Differentiator Amplifier: It is defined as an electronic circuit which provides differentiation of input applied to the Op-amp in output of the op-amp.



Due to virtual connection concept, $V_A = V_B = 0$ (Ground)
Applying KCL at node A, $I_1 = I_f$
$C_1\, d(V_i - V_A)/dt = (V_A - V_0)/ R_f$ But $V_A = 0$
$C_1\, d(V_i - 0)/dt = (0 - V_0)/ R_f$
$-V_0 / R_f = C_1\, dV_i /dt$

$$\boxed{V_0 = -C_1 R_f \frac{dV_i}{dt}}$$

Q8: Numerical: In an Op-amp, when 5 mV is applied at both the inputs of op-amp, 0.05 V is obtained. When, 5 mV and 1 mV are applied as input to the op-amp, 4.03 V is obtained. Calculate A_d , A_{CM} and CMRR in normal form and in dB form.

Solution: We know that, $V_0 = A_d V_d + A_{CM} V_{CM}$
According to first situation, $V_1 = V_2 = 5$ mV , so, $V_d = 0$ and $V_{CM} = 5$ mV
Hence, $0\, A_d + 0.005\, A_{CM} = 0.05$ Or, **$A_{CM} = 10$**
Or, A_{CM} (dB) $= 10 \log(10) = 10 \times 1$ Or, **A_{CM} (dB) = 10 dB**
According to first situation, $V_1 = 5$ mV and $V_2 = 1$ mV ,
So, $V_d = 5 - 1 = 4$ mV and $V_{CM} = (5 + 1) / 2 = 3$ mV
Hence, $0.004\, A_d + 0.003 \times 10 = 4.03$ Or, $A_d = (4.03 - 0.03)/0.004$
Or, **$A_d = 1000 = 10^3$**, Or, A_d (dB) $= 10 \log(10^3)$ Or, **A_d (dB) = 30 dB**
Hence, $A_d = 1000$ and $A_{CM} = 10$
Now, CMRR $= A_d / A_{CM} = 1000 / 10$
Or, **CMRR = 100**
CMRR (dB) $= A_d$ (dB) $- A_{CM}$ (dB) $= 30 - 10 = 20$ dB
CMRR (dB) $= 10 \log (100) = 10 \log (10^2) = 20$ dB
Hence, **CMRR = 20 dB**

Q9: Numerical: Calculate slew rate of an Op-amp if it responds a change of 1.22V at output terminal 0.61 µs after the input was changed.

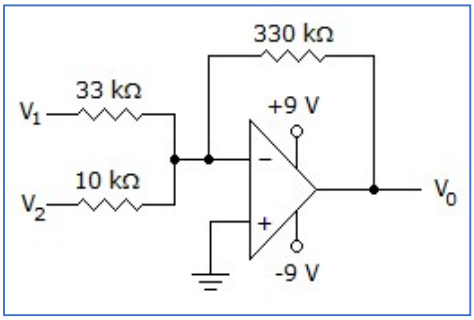
Solution: Given That

$dV_0 = 1.22$ V and $dt = 0.61$ µs

Hence Slew rate $SR = dV_0 / dt = 1.22 / 0.61$

Hence, **SR = 2 V/µs**

Q10: Numerical: Calculate the output voltage if $V_1 = -0.2$ and $V_2 = 1.1$V. (AKTU:2021-22)(5 MARKS)



Solution: We know that,

Output $V0 = -R_F V_1 / R_1 - R_f V_2 / R_2$

Hence, $V0 = -330x(-0.2)/33 - 330x1.1/10$

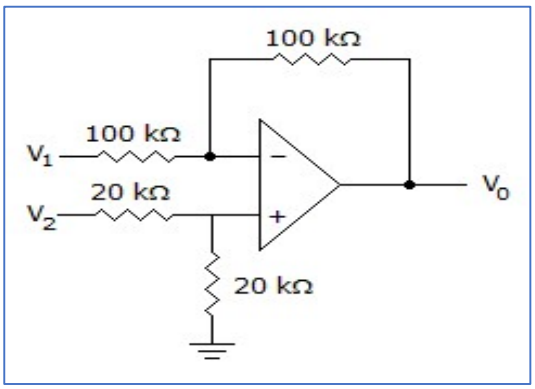
Or, $V_0 = 10x0.2 - 33x1.1$

Or, $V_0 = 2 - 36.3$ or, $V_0 = -34.3$ Volts

Since Battery potential is 9 V so output cannot exceed 9V.

Hence Output voltage will be - 9 V. (Answer = - 9V)

Q11: Numerical: Calculate the output voltage if **$V_1 = -V_2 = 2.3$ V in the given figure.**



Solution: Given $V_1 = 2.3$ V and $V_2 = -2.3$ V,

First of all, we will calculate V_B

Using voltage divider Rule,

$V_B = V_2 \times 20 / (20+20) = -2.3 \times 20 / 40 = -1.15$ Volts.

Due to virtual connection, $V_A = V_B = -1.15$ Volts.

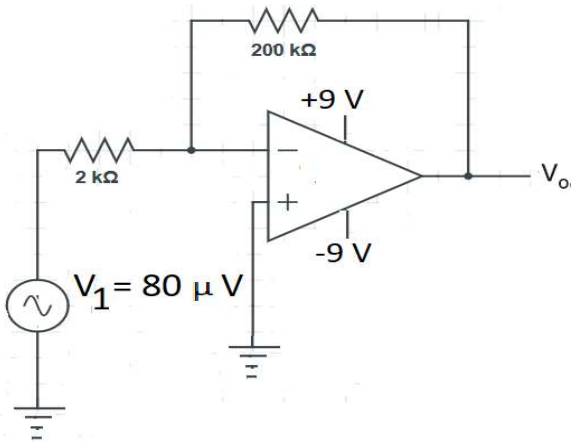
Applying KCL at node A, $I_1 = I_f$

Hence, $(V_1 - V_A)/100 = (V_A - V_0)/100$

Or, $V_0 = 2V_A - V_1 = 2 \times (-1.15) - 2.3 = -2.3 - 2.3$

Hence, **$V_0 = -4.6$ Volts.**

Q12: Numerical: Calculate the output voltage (AKTU :2020-21)(5 MARKS)



Solution: Given $V_1 = 80\ \mu V$,

Due to virtual connection, $V_A = V_B = 0$.

Applying KCL at node A, $I_1 = I_f$

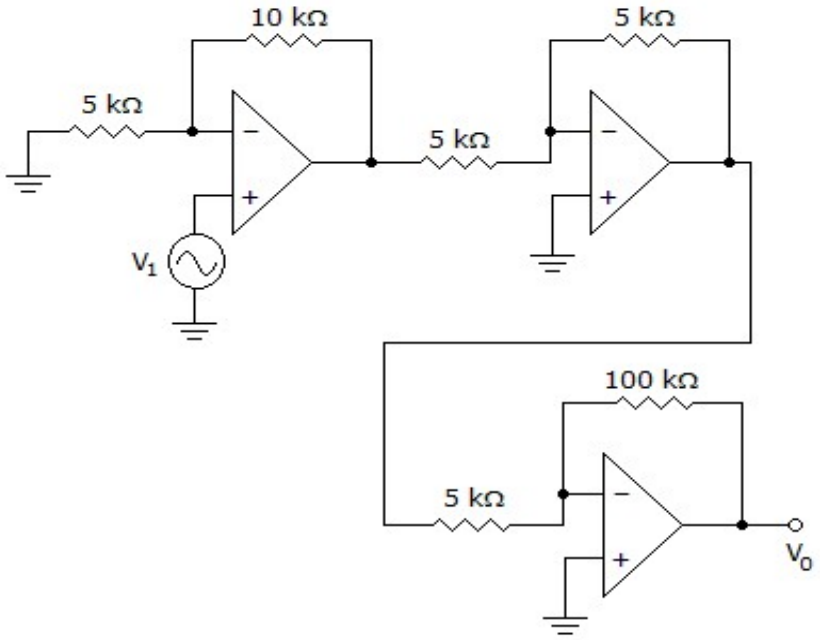
Hence, $(V_1 - V_A)/2 = (V_A - V_0)/200$

Hence, $(80 - 0)/2 = (0 - V_0)/200$

Hence, $V_0 = -80 \times 200 / 2\ \mu V = -8000\ \mu V = -8$ mV

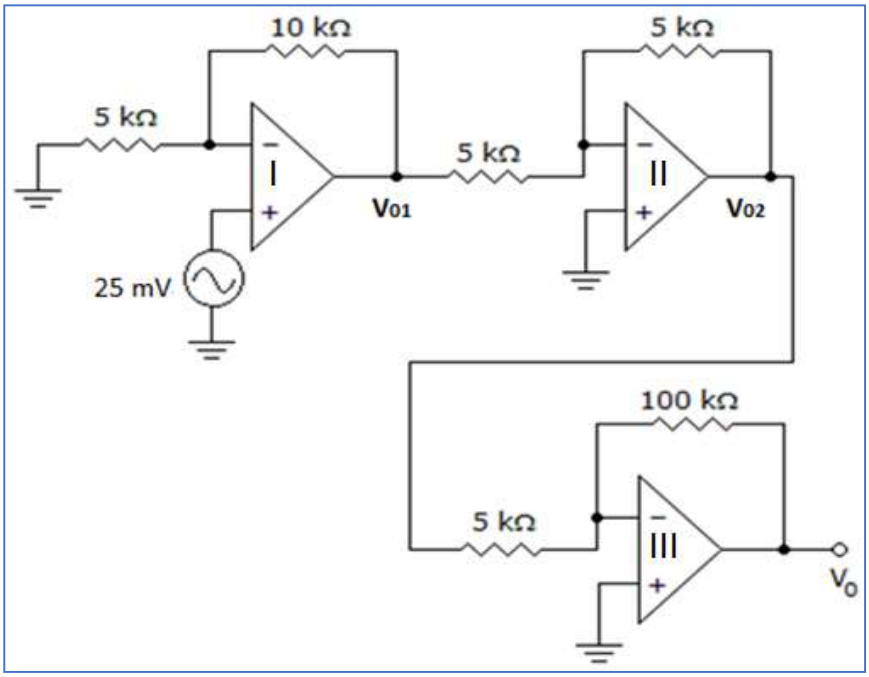
Hence **$V_0 = -8$ mV**

Q13: Numerical: Calculate V_0 when $V_1 = 25$ mV.



Solution:

Divide whole circuit into some Stage I, II, III.



For stage I:

This is a non-inverting amplifier,

Hence,

$V_{01} = (1 + R_F / R_{in}) V_{IN}$

Then $V_{01} = (1+10/5) \times 25$ mV

Or, **$V_{01} = 75$ mV**

This voltage V_{01} is used as input for Stage II.

For stage II:

This is an inverting amplifier,

Hence, $V_{02} = - R_f V_{01} / R_{in}$

Then $V_{02} = - 5 \times 75 / 5$ mV

Or, **$V_{02} = - 75$ mV**

This voltage V_{02} is used as input for Stage III.

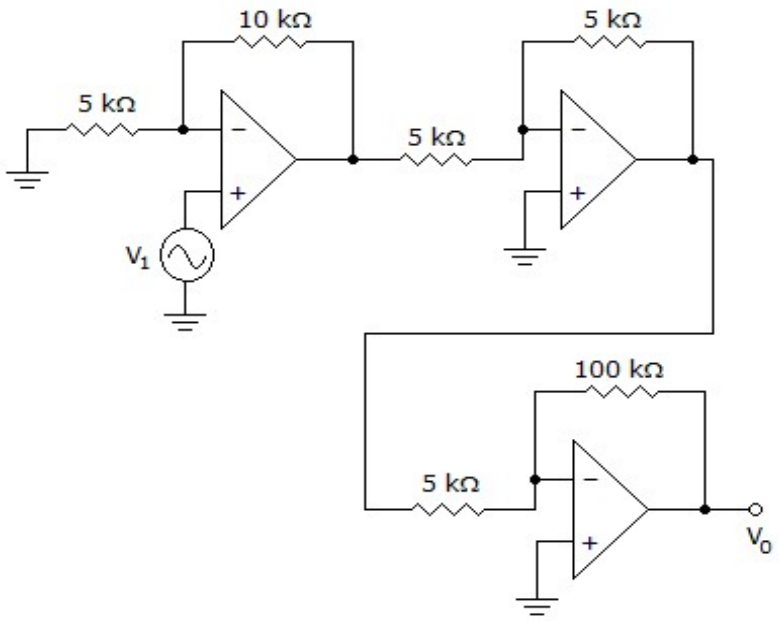
For stage III:

This is an inverting amplifier,

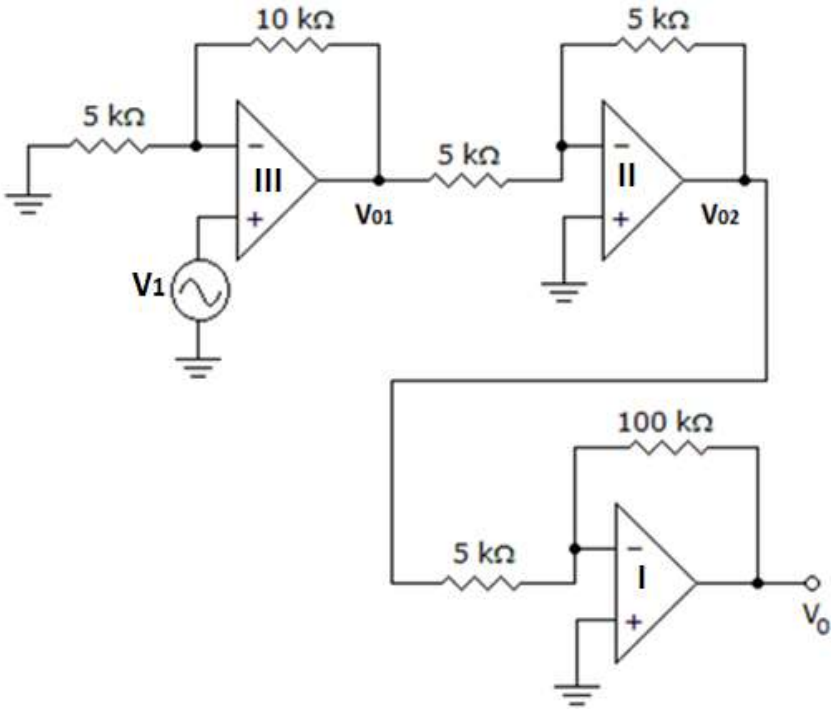
Hence, $V_0 = - R_f V_{02} / R_{in}$, Then $V_0 = - 100 \times (- 75) / 5$ mV

Or, $V_0 = 20 \times 75$ mV = 1500 mV **or, $V_0 = 1.5$ V**

Q14: Numerical: Calculate V_1 when $V_0 = 10.08$ V.



Solution: Divide whole circuit into some Stage I, II, and III.



Since Output is given and Input is to be calculated, hence, we will start with Output Stage.

For stage I:

This is an inverting amplifier,

Here input is V_{02} and output is V_0.

Hence, $V_0 = – R_f V_{02} / R_{in}$

or, $V_{02} = – R_{in} V_0 / R_f = – 5 \times 10.08 / 100 = – 50.4 / 100$ V

Hence, $\mathbf{V_{02} = – 0.504}$ **V**

For stage II:

This is an inverting amplifier, here input is V_{01} and output is V_{02}.

Hence, $V_{02} = – R_F V_{01} / R_{in}$

Or, $V_{01} = – R_{in} V_{02} / R_f$

$= – 5 \times (– 0.504)/ 5$

$= 5 \times 0.504 / 5$

Hence, **$V_{01} = 0.504$ V**

For stage III:

This is a non-inverting amplifier,

Here input is V_1 and output is V_{01}.

Hence, $V_{01} = (1 + R_F / R_{in}) V_1$

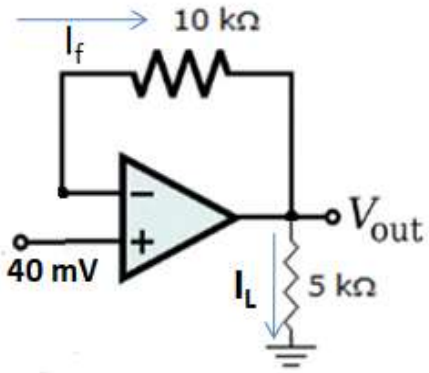
Or, $V_1 = V_{01} / (1 + R_F / R_{in})$

Or, $V_1 = 0.504 / (1 + 10/ 5)$

Or, $V_1 = 0.504 / 3$

Hence, **$V_1 = 0.168$ V**

Q15: Numerical: Calculate I_f, I_L, and V_{out} for the given circuit.



Solution: Due to virtual connection concept,

Voltages, $V_A = V_B = 40$ mV

Since input current is 0 into the Op-amp,

Applying KCL at node A , Current, **$I_f = 0$**

Or, $(V_A – V_{0ut})/ R_f = 0$ but $V_A = 40$ mA

Hence, $(40 \text{ mV} – V_{0ut})/ R_f = 0$

Hence, **$V_{0ut} = 40$ mV**

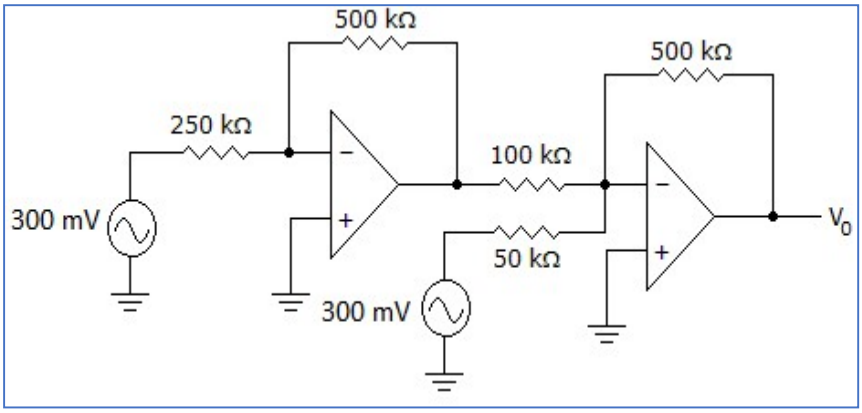
Now, load resistance = 5 kΩ

Hence, $I_L = V_{out} / R_L = 40 \text{ mV}/ 5\text{k}\Omega$

Or, **$I_L = 8$ µA**

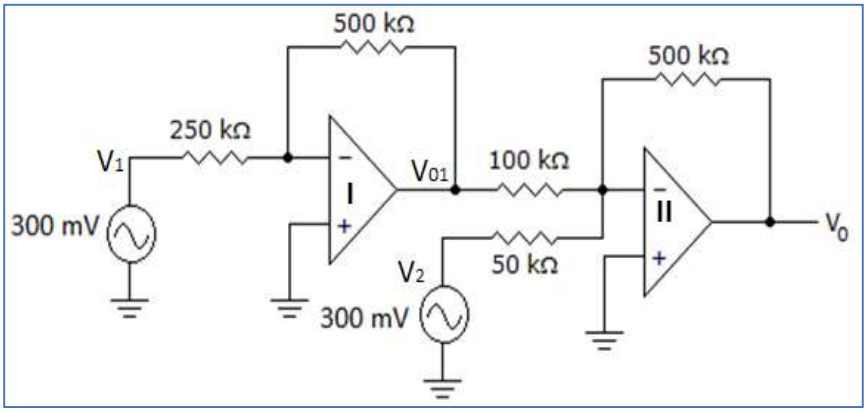
Hence, $I_f = 0$, $I_L = 8$ µA and $V_{0ut} = 40$ mV

Q16: Numerical: Calculate V_0 for the given network.



Solution:

Let us divide whole circuit into two stages I and II.



Stage I has, V_1 as input and V_{01} as output.

Stage II has, V01, and V_2 as input and V_{01} as output.

For Stage I,

This is an inverting amplifier,

Here input is V_1 and output is V_{01}.

Hence, $V_{01} = – R_F V_1 / R_{in}$

$= – 500x300/250 = – 600$ mV

For Stage II, This is an inverting summing amplifier,

Here inputs are V_2, V_{01} and output is V_0 .

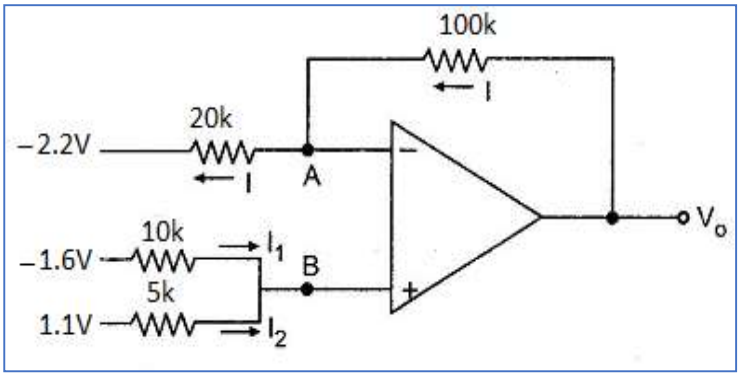
Hence, $V_0 = – R_F V_{01} / R_1 – R_F V_2 / R_2$

$= – 500x (– 600)/100 – 500x300/50$

Hence, $V_0 = + 3000 – 3000 = 0$

Hence, **$V_0 = 0$**

Q17: Numerical: Calculate V_0, I_1, I_2 and I for the given network.



Solution: To calculate V_B,

Applying KCL at node B,

$I_1 + I_2 = 0$

Or, $(-1.6 - V_B)/10 + (1.1 - V_B)/5 = 0$

Or, $-1.6 - V_B + 2.2 - 2V_B = 0$

Or, $3V_B = 0.6$ or, **$V_B = 0.2$ V**

So, $I_1 = (-1.6 - V_B)/10 = (-1.6 - 0.2) / 10 = -1.8 / 10$

Or, $I_1 = -0.18$ mA

And, $I_2 = (1.1 - V_B)/5 = (1.1 - 0.2) / 5 = 0.9 / 5$

Or, $I_2 = 0.18$ mA

Applying KCL at node A, $I_1 = I_f$

Hence, $(V_1 - V_A)/20 = (V_A - V_0)/100$

Or, $(-2.2 - 0.2)/20 = (0.2 - V_0)/100$

Or, $0.2 - V_0 = -2.4 \times 5 = -12$

Or, $V_0 = 12.2$ Volt

UNIT 4

DIGITAL ELECTRONICS

Q1: Convert Following into decimal number system:

(a) $(1101.101)_2$, (b) $(10101)_2$, (c) $(65.125)_8$, (d) $(7DF.1)_{16}$, (e) $(234.21)_5$

Sol: (a) $(1101.101)_2 = 1x2^3 + 1x2^2 + 1x2^0 + 1x2^{-1} + 1x2^{-3}$

$= 8 + 4 + 1 + 0.5 + 0.125 = (13.625)_{10}$

(b) $(10101)_2 = (1 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$

$= 16 + 0 + 4 + 0 + 1 = (21)_{10}$

(c) $(65.125)_8 = 6x8^1+5x8^0+1x8^{-1}+2x8^{-2} + 5x8^{-3}$

$= 48+5+1+0.125+0.03125+0.0097 = (54.16595)_{10}$

(d) $(7DF.1)_{16} = 7x16^2+13x16^1+15x16^0+1x16^{-1}$

$= (2015 + 0.0625) = (2015.0625)_{10}$

(e) $(234.21)_5 = 2x5^2 + 3x5^1 + 4x\ 5^0 + 2x5^{-1} + 1x5^{-2}$

$= 50 + 15 + 4 + 0.4 + 0.04 = (69.44)_{10}$

Q2: Numerical: If (24) + (17) = (40), then find the base of the numbers?

Solution: Let the base be 'r'

Then, $(24)_r + (17)_r = (40)_r$

By using representation of number

$(2xr^1 + 4x\ r^0) + (1xr^1 + 7xr^0) = 4xr^1+0xr^0$

$(2r+4)+ (r+7) =4r+0$

$3r+11 = 4r$

$4r-3r = 11$

$r = 11$ Hence, base of the given number is 11.

Q3: Numerical: If 54/ 4 = 13, then find the base of numbers.

Solution: Let the base be 'r'

$(54)_r / (4)_r = (13)_r$

$(5xr^1+ 4xr^0) / (4xr^0) = (1xr^1 + 3xr^0)$

$(5r+4)/ 4 = (r+3)$

$5r+4 = 4r+12$

$5r-4r= 12-4$

$r = 8$ Hence, base of the given number is 8.

Q4: Numerical : If x=3 & x = 6 are the roots of the quadratic equation $x^2-11x+22 = 0$, then find the base of the base of numbers?

Solution: As we know that sum of roots of quadratic equation $ax^2+bx+c = 0$, is

(-b/a)= - (Coefficient of x/ Coefficient of x^2)

From equation given, -(- 11/1) = 3 + 6 or, (11) = (9)

Let the base be 'r'

$(11)_r = (9)_r$

$(1xr^1+1xr^0) = (9xr^0)$

r +1= 9

r = 8 Hence, base of the given number is 8.

Q5: Numerical: Convert $(378.93)_{10}$ to octal.

378 to octal

8	378	
8	47	2
8	5	7
	0	5

$(378)_{10} = (572)_8$

0.93 To octal:

0.93 x 8 = 7.44	7
0.44 x 8 = 3.52	3
0.53 x 8 = 4.16	4
0.16 x 8 = 1.28	1

$(0.93)_{10} = (0.7341)_8$

Hence, $(378.93)_{10} = (572.7341)_8$

Q6: Numerical: Convert $(374 . 37)_{10}$ to hexadecimal.

378 to Hexadecimal

16	374	
16	23	6
16	1	7
	0	1

$(374)_{10} = (176)_{16}$

0.9310 to Hexadecimal :

0.37 x 16 = 5.92	5
0.92 x 16 = 14.72	E
0.72 x 16 = 11.52	B
0.52 x 16 = 8.32	8

$(0.37)_{10} = (0.5EB8)_{16}$

Hence, $(374.37)_{10} = (176.5EB8)_{16}$

Q7: Convert Octal number 372 into Binary number.

Method 1: Via Decimal Value

First convert this into decimal number:

$= (372)_8$

$= 3x8^2+7x8^1+2x8^0$

$= 3 \times 64 + 56 + 2 = 192 + 56 + 2 = (250)_{10}$

Then, convert it into binary number

$= (250)_{10}$

2	**250**	
2	125	0
2	62	1
2	31	0
2	15	1
2	7	1
2	3	1
2	1	1
	0	1

$= (11111010)_2$ which is answer.

Method 2: Direct conversion using Triplets of binary sequence

(Remember $2^3 = 8$)

First write the number

= 3 7 2

Then write their individual equivalent binary sequence in three bits each (In Triplet Form)

= 3 7 2

= 011 111 010

So, the binary sequence will be $(11111010)_2$

Q7: Convert following according to the instructions:

(i) 10,s Complement $(7634)_{10}$, (ii) 2's complement $(1101.01)_2$, (iii) 9's complement $(101.42)_{10}$, (iv) $(101.1101)_2$

(i) $(7634)_{10}$

n=4, r= 10, N= 7634

10's Compliment using formula r^n- N = 10^4- 7634 = 2366

(ii) $(1101.01)_2$

n =4, r =2, N= 1101.01

2's Compliment using formula r^n- N = 2^4- $(1101.01)_2 = (16)_{10} – (1101.01)_2$

$= (10000)_2 - (1101.01)_2 = (0010.11)_2$

(iii) $(101.42)_{10}$

Using formula, r^n-r^{-m}- N, n = 3, m= 2, N = 101.42

9's Compliment using formula r^n - r^{-m}- N = $10^3 - 10^{-2}$ - $(101.42)_{10}$

= 1000 – 0.01 – 101.42 = 998.57

(iv) $(101.1101)_2$

n= 3, m =4, N = 101.1101

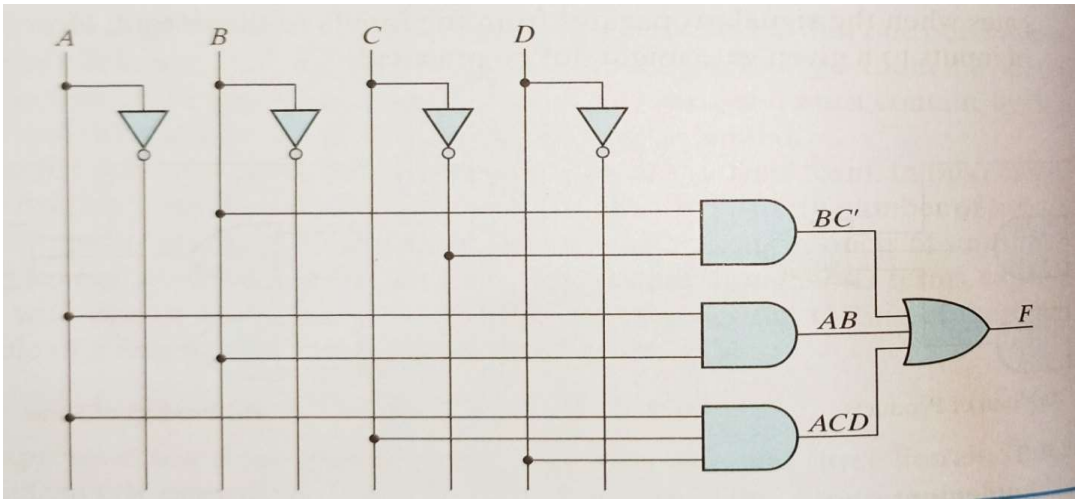
1's Compliment using formula r^n-r^{-m}- N = $(2^3 - 2^{-4})_{10} - (101.1101)_2$

= $(8 - 0.625)_{10} - (101.1101)_2 = 7.375_{10} - 101.1101_2$

= $(111.1111)_2 - (101.1101)_2 = (010.\ 0010)_2$

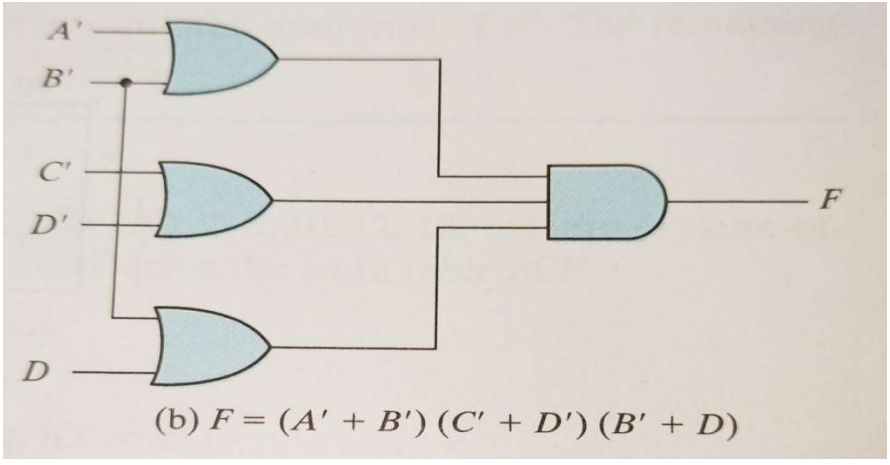
Q8: Draw a two-level logic diagram to implement the Boolean function F (A,B,C,D) = BC'+ AB+ ACD.

- **Solution:** Since the function is **SOP** therefore **AND-OR** logic will be drawn as follows:

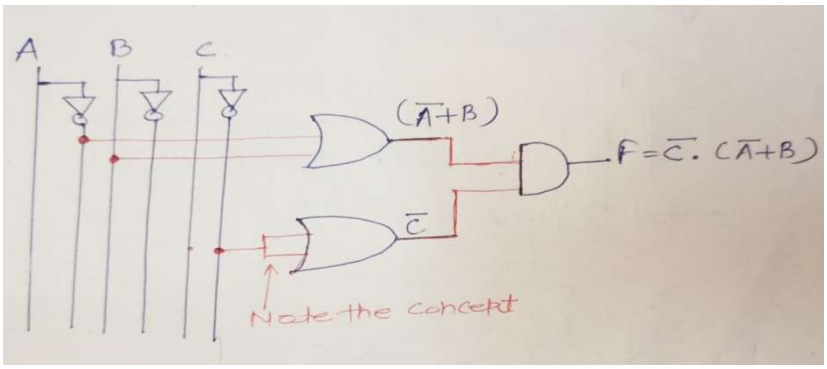


Q9: Draw a two-level logic diagram to implement the Boolean function F (A,B,C,D) = (A'+B'). (C'+D').(B'+D)

Solution: Since the function is **SOP** therefore **AND-OR** logic will be drawn as follows:



Q10: Draw the logic diagram corresponding to the following Boolean expression without simplifying it F = C'.(A'+B)



Q11: Compute $(1010100)_2 - (1000011)_2$ Using 1's Compliment

Sol:

$(1010100)_2 - (1000011)_2$ Using 1's Compliment

Solution:

(i) (1010100)+(- 1000011); (equating no of digits & can be re-written as)

(ii) (1010100)+ (1's Compliment of 1000011) ; (Always determine the compliment of the number which is negative)

(iii) 1010100 + (0111100); (1's compliment of 1010100 is 0111100)

(iv)
```
   1010100
 + 0111100   (1's compliment of 0111100)
-------------
1 0010000
```
End Carry 1

+1 (Adding this carry 1 to LSB of the sum obtained)

```
  0010001
```

Q12: Compute $(1000011)_2$ - $(1010100)_2$ Using 1's Compliment

Sol:

$(1000011)_2 - (1010100)_2$

Solution:

(i) (1000011)+ (- 1010100) ; (equating no of digits & can be re-written as)

(i) (1010100)+ (1's Compliment of 1010100) ; (Always determine the compliment of the number which is negative)

(ii) 1000011+ (0101011); (1's compliment of 1010100 is 0101011)

(iii)

	1000011	
	+ 0101011	(1's compliment of 1010100)
No End Carry	1101110	

Again determining the 1's compliment of the sum obtained

1's compliment of 1101110 is 0010001

Answer is – 0010001

Q13: $(1010100)_2 – (1000011)_2$ Using 2's Compliment

Sol:

$(1010100)_2 – (1000011)_2$ Using 2's Compliment

Solution:

(1010100) + (- 1000011) ; (equating no of digits & can be re-written as)

(1010100) + (2's Compliment of 1000011) ; (Always determine the compliment of the number which is negative)

1010100 + (0111100); (2's compliment of 1000011 is 0111101)

	1010100	
	+ 0111101	(1's compliment of 0111100)
Discard End Carry	**1** 0010001	

Answer: 0010001

Q14: $(1000011)_2 - (1010100)_2$ Using 2's Compliment

Sol:

$(1000011)_2 - (1010100)_2$ Using 2's Compliment

Solution:

(i) (1000011)+ (- 1010100) ; (equating no of digits & can be re-written as)

(ii) (1010100)+ (2's Compliment of 1010100) ; (Always determine the compliment of the number which is negative)

(iii) 1000011+ (0101011); (2's compliment of 1010100 is 0101100)

(iv)

	1000011	
	+ 0101100	(1's compliment of 1010100)
No End Carry	1101111	

Again determining the 2's compliment of the sum obtained

2's compliment of 1101110 is 0010001

Answer: - 0010001 (Placing –ve sign in front as 1000011 < 1010100)

Q15: $(72532)_{10} - (3250)_{10}$ using 9's compliment

Sol:

$(72532)_{10} - (3250)_{10}$ **using 9's compliment**

Solution:

(72532)+ (- 03250) ; (equating no of digits & can be re-written as)

(72532)+ (9's Compliment of 03250) ; (Always determine the compliment of the number which is negative)

72532 + (96749); (9's compliment of 03250 is 96749)

```
   72532
 + 96749   (9's compliment of 03250)
 69281
```

End Carry 1

+1 (Adding the End carry to LSD OF sum obtained)

69282

Q16: $(3250)_{10} - (72532)_{10}$ Using 9's Compliment

Sol:

$(3250)_{10} - (72532)_{10}$ **Using 9's Compliment**

Solution:

(i) (03250) + (-72532);

(ii) (03250)+ (9's Compliment of 72532) ;

(iii) (03250 + (27467); (9's compliment of 03250 is 96749)

(iv)

```
   03250
 + 27467   (9's compliment of 03250)
 30717
```

No End Carry

Again determining the 9's compliment of the sum obtained

```
   99999
  -30717
   69282
```

Answer: - 69282

Q17: $(72532)_{10} - (3250)_{10}$ using 10's compliment

Sol:

$(72532)_{10} - (3250)_{10}$ **using 10's compliment**

Solution:

(i) (72532)+ (- 03250) ; (equating no of digits & can be re-written as)

(ii) (72532)+ (10's Compliment of 03250) ; (Always determine the compliment of the number which is negative)

(iii) 72532 + (96750); (10's compliment of 03250 is 96750)

(iv)

```
   72532
 + 96750   (10's compliment of 03250)
1 69282
```

Discard End Carry

69282 **Answer**

Q18: $(3250)_{10} - (72532)_{10}$ Using 10's Compliment

Sol:

$(3250)_{10} - (72532)_{10}$ **Using 10's Compliment**

Solution:

(i) (03250) + (-72532); (equating no of digits & can be re-written as)

(ii) (03250)+ (10's Compliment of 72532) ; (Always determine the compliment of the number which is negative)

(iii) (03250 + (27468); (10's Compliment of 72532 is 27468)

(iv)

```
    03250
+ 27468   (10's Compliment of 72532)
-------
  30718
```

No End Carry

Again determining the 9's compliment of the sum obtained

```
  99999
- 30718
-------
  69282
```

Answer: - 69282

Q19: Numerical: Convert F(A,B,C) = (A+B).(A+C).(B+C') into canonical form.

Solution: F(A,B,C) = (A+B).(A+C).(B+C')

We know that AA' = BB' = CC' = 0

Hence put Anyone of these at the place of missing term. Hence,

F(A,B,C) = (A+B+CC').(A+C+BB').(B+C'+AA')

= (A+B+C).(A+B+C').(A+C+B).(A+C+B').(B+C'+A).(B+C'+A')

= (A+B+C).(A+B+C').(A+B'+C).(A'+B+C')

= ∏M(0, 1, 2, 5)

Q20: Numerical: Convert F(A,B,C) = AB + AC' + BC into canonical form.

Solution: F(A,B,C) = AB + AC' + BC

In AB, C is missing; hence multiply it with (C + C').

In AC', B is missing; hence multiply it with (B + B').

In BC, A is missing; hence multiply it with (A + A').

F(A,B,C) = AB + AC' + BC

= AB(C + C') + AC'(B + B') + BC(A + A')

= ABC + ABC' + ABC' + AB'C' + ABC + A'BC

= ABC + ABC' + AB'C' + A'BC

Or, F(A,B,C) = A'BC + AB'C' + ABC' + ABC

= Σm(3, 4, 6, 7)

Q21: Minimize Boolean expression Q = ABC + A(B'+C')

Solution: Q = ABC + A(B'+C')

= ABC + AB' + AC'

= ABC + AB'(C + C') + AC'(B + B')

= ABC + AB'C' + AB'C + AB'C' + ABC'

= ABC + AB'C' + AB'C + ABC'

= ABC + ABC’ + AB’C’ + AB’C

= AB (C + C’) + AB’(C + C’) But C + C’ = 1

= AB + AB’

= A(B + B’) But B + B’ = 1

So, **Q = A**

Q22: Minimize Boolean expression Q = A'BC' + AB'C' + AB'C + ABC' + ABC

Solution: Q = A'BC‘ + ABC' + AB'C' + AB'C + ABC' + ABC

[∵ ABC+ABD=AB(C+D)]

= (A‘+A)BC' + AB'(C+C') + AB(C+C')

[∵ A'+A=C’+C=1]

= BC' + AB' + AB

= BC' + A(B'+B)

[∵ B'+B=1]

= BC' + A

Hence, **Q = BC' + A**

Q23: Minimize Boolean expression using truth table.

Q = (A+B+C).(A+B+C').(A+B'+C')

Solution: Q = (A+B+C).**(A+B+C')**.(A+B'+C')

= (A+B+C).(A+B+C').(A+B+C').(A+B'+C')

= [(A+B) + CC’] . [(A+C') + BB’]

[∵ BB’ = CC' = 0]

= (A+B).(A+C')

[∵ (A+B).(A+C) = A +BC]

= A +BC’

Hence, Q = A +BC’

Q24: Minimize Boolean expression using truth table.

Q = (A+B+C).(A+B+C')

Solution: Q = (A+B+C).(A+B+C')

= (A+B)+(CC')

[∵ CC' = 0]

= (A+B)

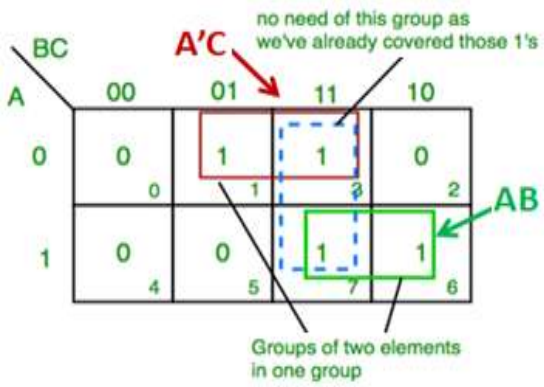
Hence, Q = A + B

Q25: Numerical: Simplify the following Boolean function,

Z= ∑A,B,C(1,3,6,7) using K-map.

Solution: Z= ∑A,B,C(1,3,6,7)

It is a three variable function. Hence, number of cells will be $2^3 = 8$.



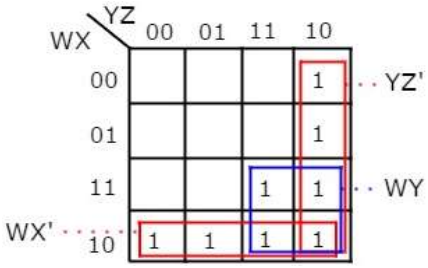
From red group we get product term —**A'C**

From green group we get product term — **AB**

Summing these product terms, we get-Final expression Z **= (A'C + AB)**

Q26: Numerical: Simplify the following Boolean function, **f(**W,X,Y,Z)**= WX'Y' + WY + W'YZ'** using K-map.

Solution: f = ∑m(2,6,8,9,10,11,14,15)

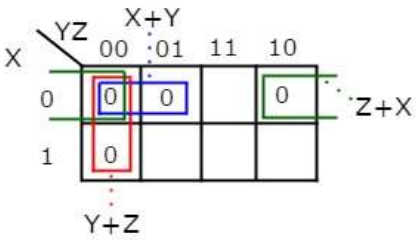


We got three prime implicants WX', WY & YZ'.

Hence, Minimized **f = WX' + WY + YZ'**

Q27: Numerical: Simplify the following Boolean function, f(X,Y,Z) = ∏M (0,1,2,4) using K-map.

Solution: f(X,Y,Z) = ∏M (0,1,2,4)



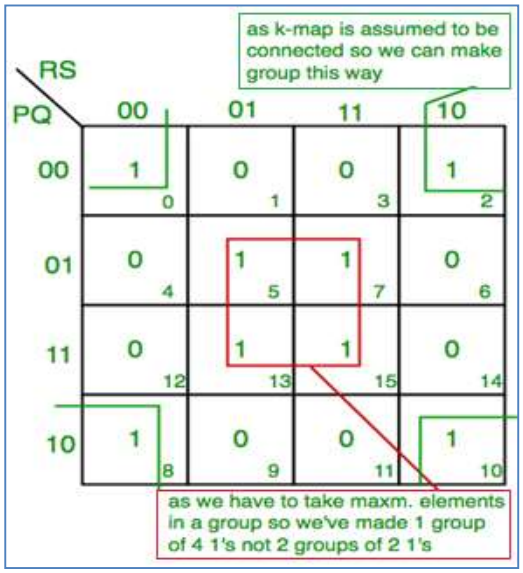
We got three prime implicants X+Y, Y+Z & Z+X. All these prime implicants are **essential** because one zero in each grouping is not covered by any other groupings except with their individual groupings.

Hence, **f = (X+Y).(Y+Z).(Z+X)**

Q28: Numerical: Simplify the following Boolean function, F(P,Q,R,S)=∑(0,2,5,7,8,10,13,15) using K-map.

Solution: F(P,Q,R,S)=∑(0,2,5,7,8,10,13,15)

It is a four variable function. Hence, number of cells will be 2^4 = 16.



From **red** group we get product term — **QS**

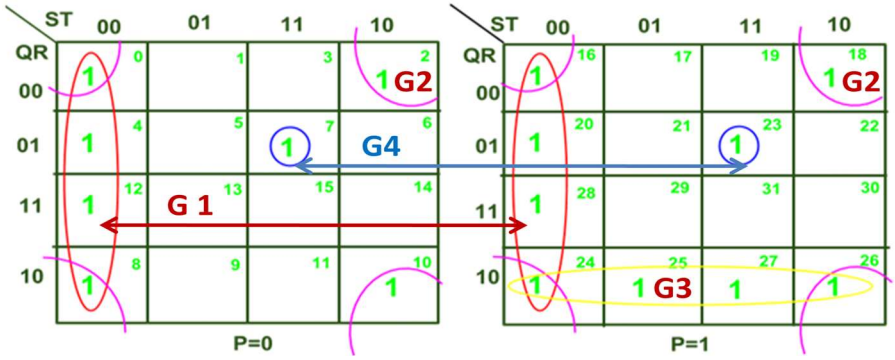
From **green** group we get product term — **Q'S'**

Summing these product terms we get- Final expression **F = (QS+Q'S')**

Q29: Numerical: Simplify the following Boolean function,

F=∑m(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28) using K-map.

Solution: F=∑m(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28), we know that $2^5 = 32$, Hence, number of variables are 5 here.



G 1: The one marked in red comprises of cells (0, 4, 8, 12, 16, 20, 24, 28),

G 2: The one marked in pink comprises of cells (0, 2, 8, 10, 16, 18, 24, 26),

G 3: The one marked in yellow comprises of cells (24, 25, 26, 27) ,

G 4: The one marked in blue comprises of cells (7, 23)

G 1: S'T' G 2: R'T' G 3: PQR' G 4: Q'RST

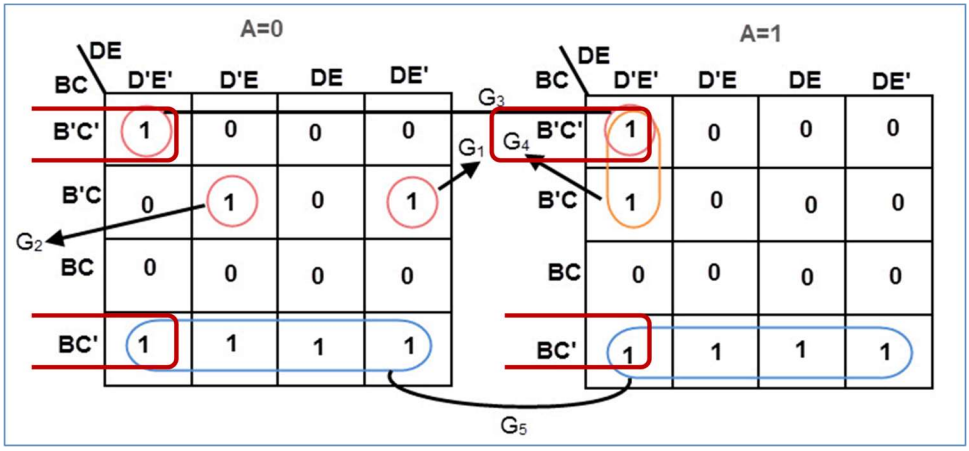
Hence, final answer is **F = S'T' + R'T' + PQR' + Q'RST**

Q30: Numerical: Simplify the following Boolean function using K-map.

f (A, B, C, D, E) = ∑ m (0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27)

Solution: f (A, B, C, D, E) = ∑ m (0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27) ,

Since, number of variables are 5 here, hence number of cells $2^5 = 32$.

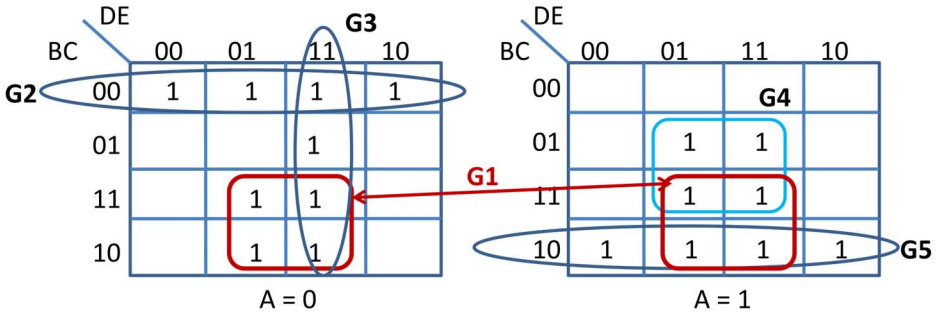


f = A'B'CDE' + A'B'CD'E + C'D'E' + AB'D'E' + BC'

Q31: Numerical: Simplify Y = ∑m (0, 1, 2, 3, 7, 9, 11, 13, 15, 21, 23, 24, 25, 26, 27, 29, 31) using K Map.

Solution: Y = ∑m(0,1,2,3,7,9,11,13,15,21,23,24,25,26,27,29,31)

Number of cells = 32 = 2^5 , Hence, number of variables = 5 (A,B,C,D,E)

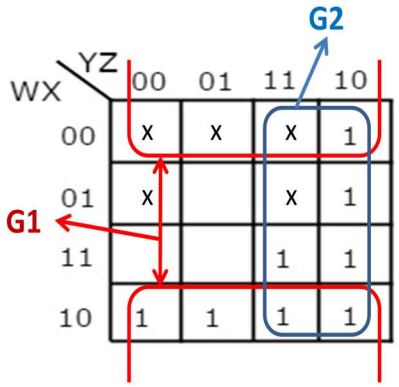


Hence, **Y = BE+A'B'C'+A'DE+ACE+ABC'**

Q32: Numerical: Simplify the following Boolean function,

f(W,X,Y,Z) = ∑m(2,6,8,9,10,11,14,15) + ∑d(0,1,3,4,7) using K-map.

Solution: f = ∑m(2,6,8,9,10,11,14,15) + ∑d(0,1,3,4,7)



1. G1: m(0,1,2,3,8,9,10,11)

2. G2: m(3,4,6,7,10,11,14,15)

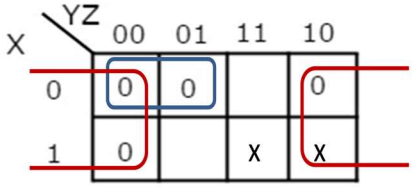
We got two prime implicants X' and Y. All these prime implicants are essential.

Hence, Minimized **f = X' + Y**

Q33: Numerical: Simplify the following Boolean function,

f(X,Y,Z) = ∏M (0,1,2,4) + ∏d (6,7) using K-map.

Solution: f(X,Y,Z)=∏M(0,1,2,4)

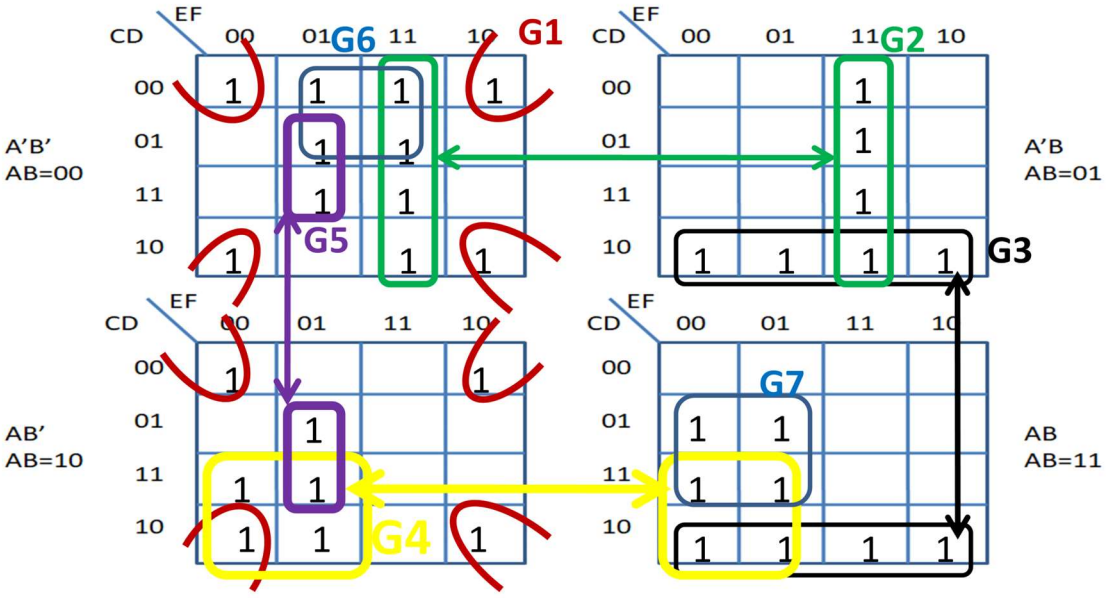


We got three prime implicants Z and X + Y. One don't care is used as 0 and others is not used because it is not needed to be grouped.

Hence, **f = (X+Y).Z**

Q34: Numerical: Simplify Y = ∑m(0,1,2,3,5,7,8,10,11,13,15,19,23,24,25,26,27, 31,32,34,37,40,41,42,44,45,52,53,56,57,58,59,60,61) using K Map.

Solution:



Answer: **Y = B'D'F'+A'EF+BCD'+ACE'+B'DE'F+A'B'C'F+ABDE'**

UNIT – 5

Ques 1. What is RADAR? Write down two applications of RADAR. (2 marks) (2021-22)

Sol.

RADAR (Radio Detection and Ranging): The full form of RADAR is Radio Detection and Ranging. Detection refers to whether the target is present or not. The target can be stationary or movable, i.e., non-stationary. Ranging refers to the distance between the Radar and the target.

Radars can be used for various applications on ground, on sea and in space. The **applications** of Radars are listed below.

- Controlling the Air Traffic
- Ship safety
- Sensing the remote places
- Military applications

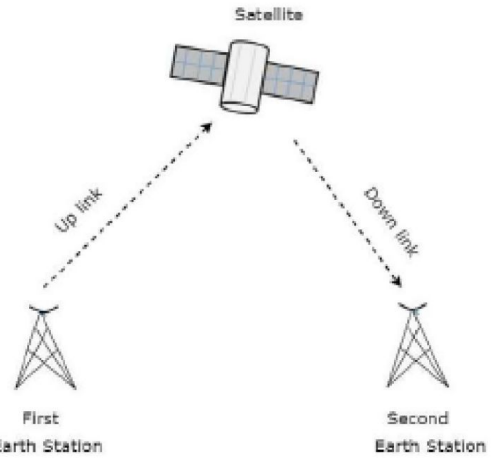
Ques 2. Describe briefly satellite communication. (5 marks) (2021-22)

Sol.

Satellite Communication: Communication refers to the exchange (sharing) of information between two or more entities, through any medium or channel. In other words, it is nothing but sending, receiving and processing of information. If the communication takes place between any two earth stations through a satellite, then it is called as satellite

Need of Satellite Communication: Different kinds of propagations (Ground wave Propagation, Space wave propagation) are used earlier for communication up to some distance. Satellite Communication provides **communication for long distances**, which is well beyond the line of sight.

How a Satellite works:



A **repeater** is a circuit, which increases the strength of the received signal and then transmits it. But, this repeater works as a **transponder**. That means, it changes the frequency band of the transmitted signal from the received one.

The transmission of signal from first earth station to satellite through a channel is called as **uplink** and the frequency is **Uplink frequency**. Similarly, the transmission of signal from satellite to second earth station through a channel is called as **downlink** and the frequency is **Downlink frequency**. In similar way, second earth station can also communicate with the first one.

The process of satellite communication begins at an earth station. Here, an installation is designed to transmit and receive signals from a satellite in an orbit around the earth. Earth stations send the information to satellites in the form of high powered, high frequency (GHz range) signals.

Ques 3.

An audio frequency signal $5Sin(2\pi\times500t)$ is used to amplitude modulate a carrier of $25Sin(2\pi\times10^5t)$. Calculate:

(i) Modulation index
(ii) Amplitude of Each side band

(iii) Total power
(iv) Bandwidth
(v) Transmission efficiency

(10 marks) (2021-22)

Sol.

(i) $\mu = a_m = \frac{A_m}{A_c} = \frac{5}{25} = 0.2$

(ii) Amplitude of each sideband $= \frac{m_a \cdot V_c}{2}$

$= \frac{0.2\times25}{2} = 2.5$

(iii) Total Power, $P_T = P_c\left(1+\frac{m_a^2}{2}\right)$

$= \frac{(25)^2}{2\times1}\left(1+\frac{0.2^2}{2}\right)$

$= \frac{625}{2}(1+0.02)$

$= 312.5\times1.02$

$= 318.75$ Watt

(iv) Bandwidth $= 2f_m$

$= 2\times500 = 1\,kHz$

(v) Transmission Efficiency $= \frac{m_a^2}{2\left(1+\frac{m_a^2}{2}\right)}$

$= \frac{(0.2)^2}{2\left(1+\frac{(0.2)^2}{2}\right)}$

$= \frac{0.04}{2\times1.02}$

$= \frac{0.04}{2.04} = 1.9\%$

Ques 4. Enlist the merits of satellite communication.(2 marks) (2021-22)

Sol.

1. Design, development, investment, and insurance of satellite requires higher cost.
2. There can be a congestion of frequencies.
3. propagation issues and interference may arise.
4. Launching satellites into orbit is an expensive process.

Ques 5. Explain Amplitude modulation. Derive the expression for the total power radiated by the modulated signal. Also calculate modulation efficiency. (10 marks) (2021-22)

SOL.

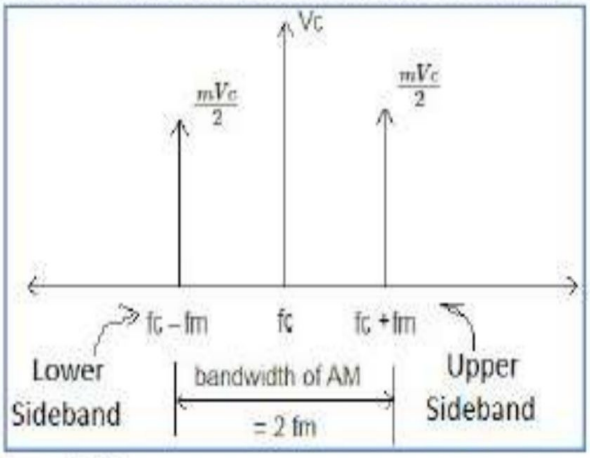
Modulation: Modulation is the process or technique by which a low frequency signal (or **modulating signal** or baseband signal), is superimposed on a high frequency signal (or **carrier signal**) for increasing transmission range of the signal.

OR

Modulation is the process or technique by which any one parameter (Amplitude, Frequency or Phase) of the **carrier signal** is changed in accordance with the **modulating signal** for increasing transmission range of the signal.

a) If Amplitude of carrier signal is changed according to the modulating signal, **Amplitude Modulation** occurs.
b) If Frequency of carrier signal is changed according to the modulating signal, **Frequency Modulation** occurs.
c) If Phase of carrier signal is changed according to the modulating signal, **Phase Modulation** occurs.

Amplitude Modulation: Amplitude Modulation is the process or technique by which Amplitude of the **carrier signal** is changed in accordance with the **modulating signal** for increasing transmission range of the signal.



The amplitude of Upper Sideband = $m_a V_c/2$

The amplitude of Lower Sideband = $m_a V_c/2$

The amplitude of Central Band = V_c

As Power Content in a wave = V_{rms}^2/R

Hence, Carrier Power $P_c = (V_c/\sqrt{2})^2/R = V_c^2/2R$

Upper Sideband Power $P_{USB} = (m_a V_c/2\sqrt{2})^2/R = m_a^2 V_c^2/8R$

And, Lower Sideband Power $P_{LSB} = (m_a V_c/2\sqrt{2})^2/R = m_a^2 V_c^2/8R$

Hence, Total Sideband Power $P_{SB} = 2m_a^2 V_c^2/8R = m_a^2 V_c^2/4R$

Hence, total power content in AM wave

$P_t = P_c + P_{USB} + P_{LSB} = P_c + P_{SB}$

Here, $P_c = V_c^2/2R$ and $P_{SB} = m_a^2 V_c^2/4R = P_c m_a^2/2$

Or, $P_t = P_c + P_{SB}$

Or, $P_t = P_c + P_c m_a^2/2$

Or, $P_t = P_c (1 + m_a^2/2)$ Hence,

Ques 6. Why do we need modulation? The antenna current of an AM transmitter is 8 A when only the carrier is sent, but it increases to 8.93 A, when the carrier is modulated by a single sine wave. Find percentage modulation. Determine the antenna current when the percent of modulation changes to 0.8.

Sol.

Need of Modulation: Modulation is needed due to following reasons:

1 – Communication range of low frequency signals is very low.

2 – Occurrence of interference is more in low frequency signals.

3 – Power consumption increases using low frequency signal for large transmission range.

4 – Antenna height for transmitting a low frequency signal is very large (in order of kms) which is not feasible. Antenna height for any transmission is $l = \lambda/4$.

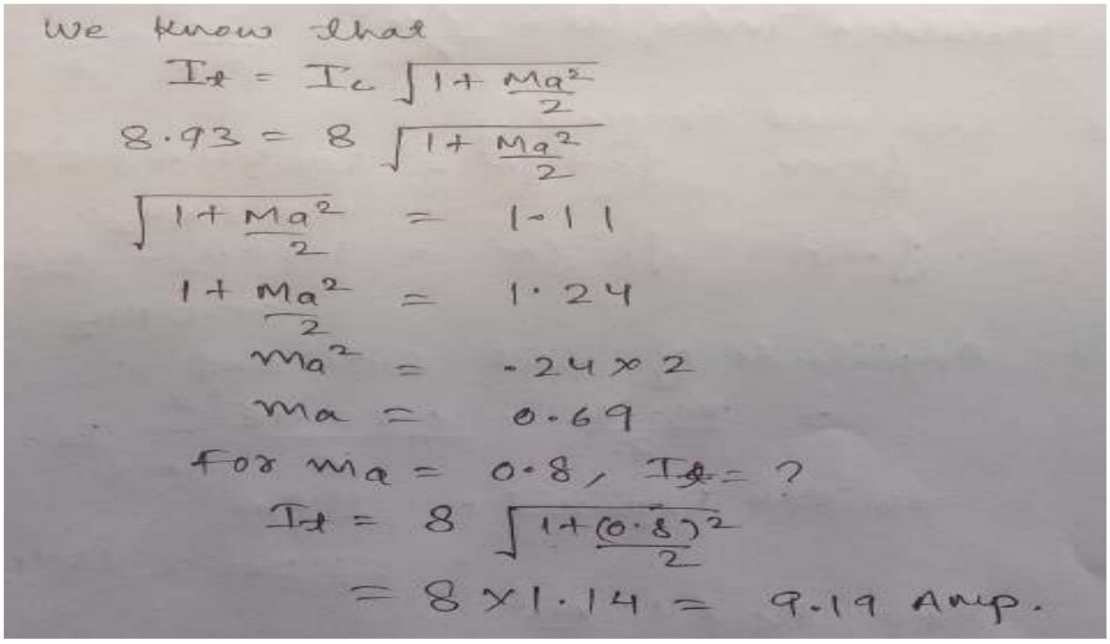
a) Suppose a low frequency $f_1 = 3kHz$, Hence $\lambda = c/f = 3x10^8/(3x10^3)$

Or, $\lambda = 10^5$ meter = 10 kms, Hence $l = \lambda/4 = 2.5Kms$ **(Not Feasible)**

b) Suppose a high frequency $f_2 = 3GHz$, Hence $\lambda = c/f = 3x10^8/(3x10^9)$

Or, $\lambda = 0.1$ meter = 10 cm, Hence $l = \lambda/4 = 2.5$ cm **(Feasible)**

Hence modulation is needed.



Ques7.

An Audio frequency signa10 Sin $6\pi \times 400t$ is used to amplitude modulate a carrier of 25 sin $4\pi \times 10^5 t$. Calculate

(i) Modulation Index
(ii) Amplitude of each side band
(iii) Total power delivered to the load of 2KΩ
(iv) Bandwidth
(v) Transmission efficiency

Sol.

(i) Modulation index, $\mu = \frac{A_m}{A_c} = \frac{10}{25} = 0.4$

(ii) Amplitude of each side band $= \frac{m_a \cdot V_c}{2}$

$= \frac{0.4 \times 25}{2}$

$= 5$

(iii) Total power delivered to 2kΩ

$P_t = P_c\left(1 + \frac{m_a^2}{2}\right)$

where $P_c = \frac{V_c^2}{2R}$

$P_t = \frac{(25)^2}{2}\left(1 + \frac{0.4^2}{2}\right)$

$= \frac{625}{2 \times 2^3}\left(1 + \frac{0.16}{2}\right)$

$= 312.5 \times 1.08 \times 10^{-3}$

$= 337.5$ Watt

$= 0.3375$ Watt.

(iv) Bandwidth $= 2 f_m$

$= 2 \times 1200 = 2400$ Hz

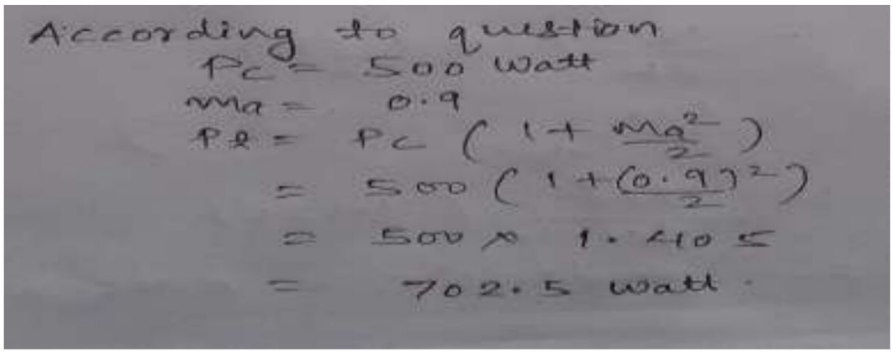
$= 2.4$ kHz

(v) Transmission efficiency $= \frac{m_a^2}{2\left(1 + \frac{m_a^2}{2}\right)}$

$= \frac{(0.4)^2}{2\left(1 + \frac{0.4^2}{2}\right)} = \frac{0.16}{2 \times 1.08}$

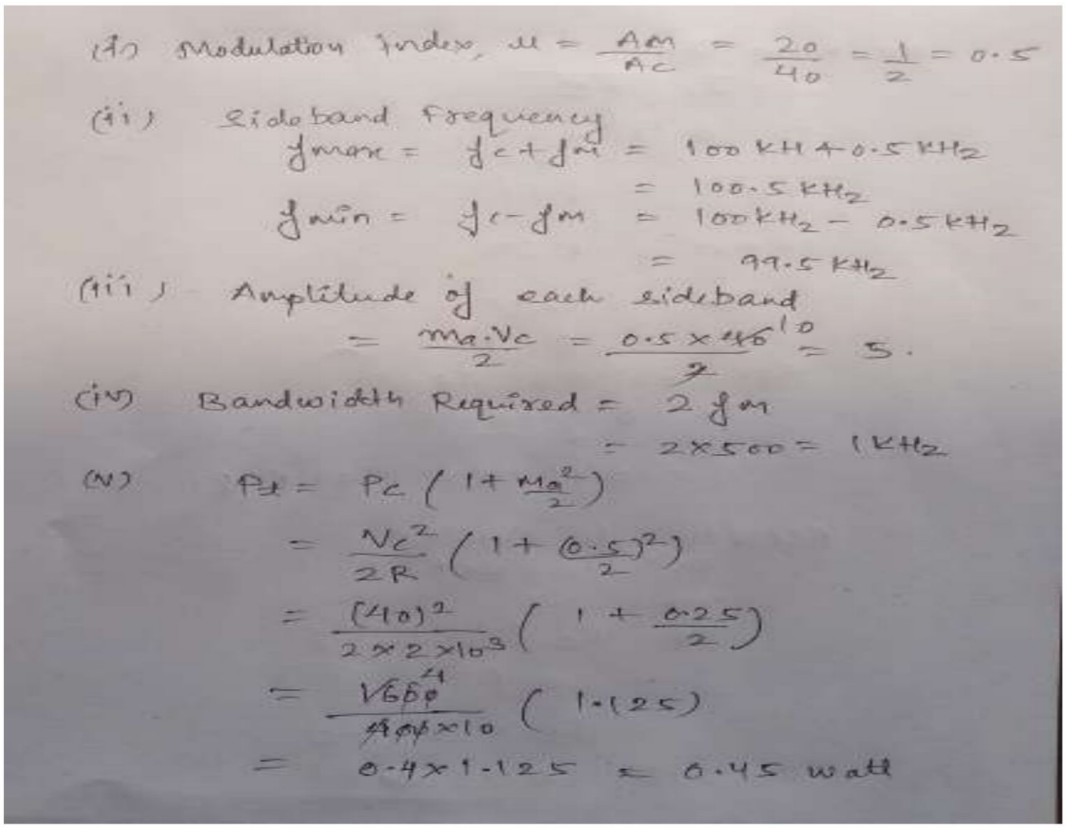
$= 7.9$

Ques 8. 500 watt carrier power is modulated to depth of 90%, calculate the total power in the modulated wave.(2 marks) (2022-23)
Sol.



Ques 9.
An audio frequency signal 20 Sin 2 π x 500 t is used to amplitude modulated a carrier of 40 Sin 2 π x 10^5 t.
Calculate :
(i) Modulation Index (ii) Sideband Frequency (iii) Amplitude of each sideband (iv) Bandwidth required (v) Total power delivered to the load of 2 KΩ

Sol.



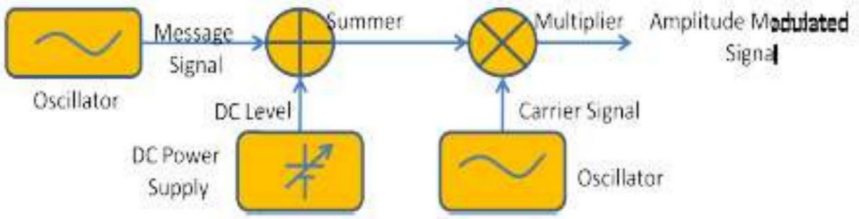
Ques 10. (i) Describe AM modulator with adequate diagram. (7 marks) (2022-23)
(ii) Explain the elements of communication system with the help of block diagram.
Sol.

Amplitude Modulation Techniques:

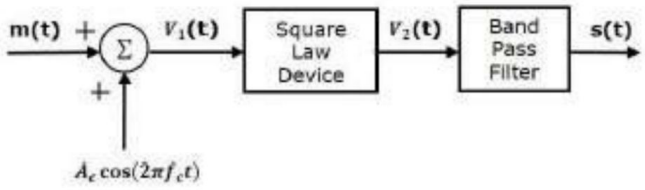
High level modulator: A high level modulator is defined as one that modulates a high power section of the circuit, typically the final RF amplifier. It has the advantage that linear amplifiers are not required for the RF amplification stages after AM modulation has been applied. The drawback is that high power audio amplifiers are needed. For broadcast transmitters where very high power levels are used, class D or class E amplifiers may be employed for the audio output.

Low level modulator: A low level AM modulator would be one where the modulation is applied to low power stage of the transmitter, typically in the RF generation stages, or via the digital signal processing areas. The drawback of this approach is that linear amplification is required for the RF stages.

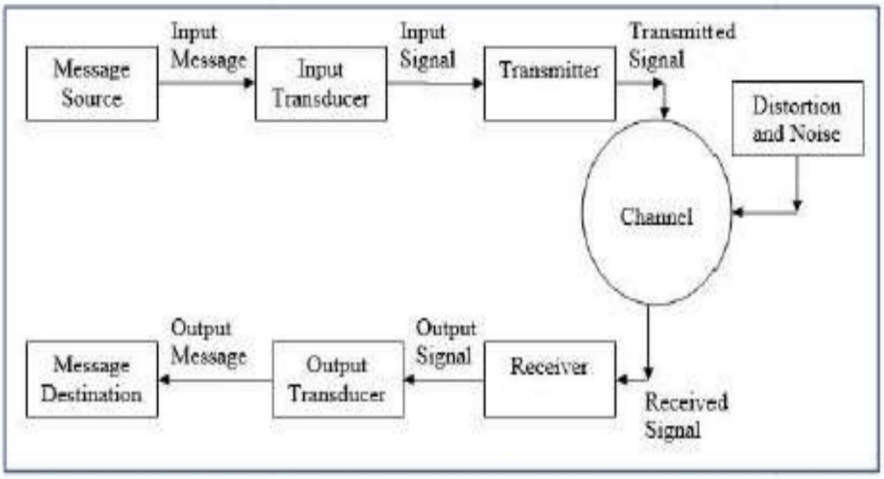
Amplitude Modulation Techniques: General Way: AM generation involves mixing of a carrier and an information signal. In low level modulation, the message signal and carrier signal are modulated at low power levels and then amplified. The advantage of this technique is that a small audio amplifier is sufficient to amplify the message signal.
From the equation, $am(t) = A_c [1 + m_a \cos w_m t] \cos w_c t$
We require, an summer where modulation signal is summed to a DC level and then multiplied to carrier signal.



Nonlinear Square Law AM modulator: Let the modulating and carrier signals be denoted as m(t) and $A_c \cos(2\pi f_c t)$ respectively. These two signals are applied as inputs to the summer (adder) block. This summer block produces an output, which is the addition of the modulating and the carrier signal.



Communication Systems: The communication system is a system which describes the information exchange between two points. The process of transmission and reception of information is called **communication**. The major elements of **communication** are the Transmitter of information, Channel or medium of **communication** and the Receiver of information.



Elements of Communication Systems:

Message Source: It generates or originates messages. **For Example:** Our Mouth

Input Message: This is the information which is to be sent to destination. **For Example:** Voice signal generated from mouth

Input Transducer: It converts the input message into electrical form. The signal can be processed in electrical form. **For example:** Mic

Input Signal: The data in electrical form (this is a baseband signal). It is a low frequency signal, also known as modulating signal. **For Example:** Voice Signal into electrical form

Transmitter: It modifies the signal for transmission (amplifies, modulates) and transmits it.

Channel: It is the medium over which the transmitted signal is sent. It can be wired (Optical fiber, wires, coaxial cable) or wireless (air, space in electromagnetic form or in light form).

Distortion/Noise: It is the external signals/features that affect the signal. This is added through channel, in the signal to be sent and distorts it. The process of adding unwanted signal is **Interference**.

Receiver: It modifies the received signal (amplifies and demodulates it). For Example: Voice signal in electrical form

Output Transducer: It converts message from electrical signal back into its original form in which form, it was generated. **For Example:** Speaker converts electrical signal in voice form

Output Message: The message which is received at destination end. **For Example:** Our voice signal

Message Destination: It receives the signal sent from source. **For Example:** Our Ears.

Components of a signal:

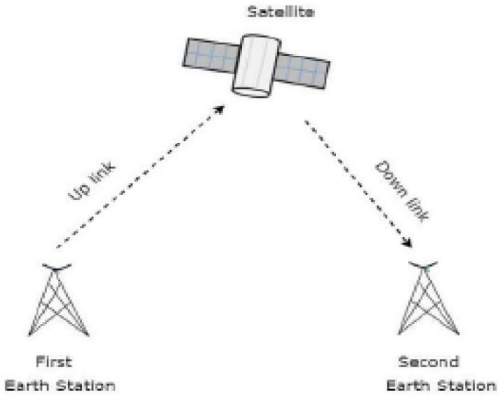
Ques 11. Explain the satellite and radar system using proper block diagram.(7 marks) (2022-23)

Sol.

Satellite Communication: Communication refers to the exchange (sharing) of information between two or more entities, through any medium or channel. In other words, it is nothing but sending, receiving and processing of information. If the communication takes place between any two earth stations through a satellite, then it is called as **satellite**

Need of Satellite Communication: Different kinds of propagations (Ground wave Propagation, Space wave propagation) are used earlier for communication up to some distance. Satellite Communication provides **communication for long distances**, which is well beyond the line of sight.

How a Satellite works:



A **repeater** is a circuit, which increases the strength of the received signal and then transmits it. But, this repeater works as a **transponder**. That means, it changes the frequency band of the transmitted signal from the received one.

The transmission of signal from first earth station to satellite through a channel is called as **uplink** and the frequency is **Uplink frequency**. Similarly, the transmission of signal from satellite to second earth station through a channel is called as **downlink** and the frequency is **Downlink frequency**. In similar way, second earth station can also communicate with the first one.

The process of satellite communication begins at an earth station. Here, an installation is designed to transmit and receive signals from a satellite in an orbit around the earth. Earth stations send the information to satellites in the form of high powered, high frequency (GHz range) signals.

RADAR (Radio Detection and Ranging): The full form of RADAR is Radio Detection and Ranging. Detection refers to whether the target is present or not. The target can be stationary or movable, i.e., non-stationary. Ranging refers to the distance between the Radar and the target.

Radars can be used for various applications on ground, on sea and in space. The **applications** of Radars are listed below.

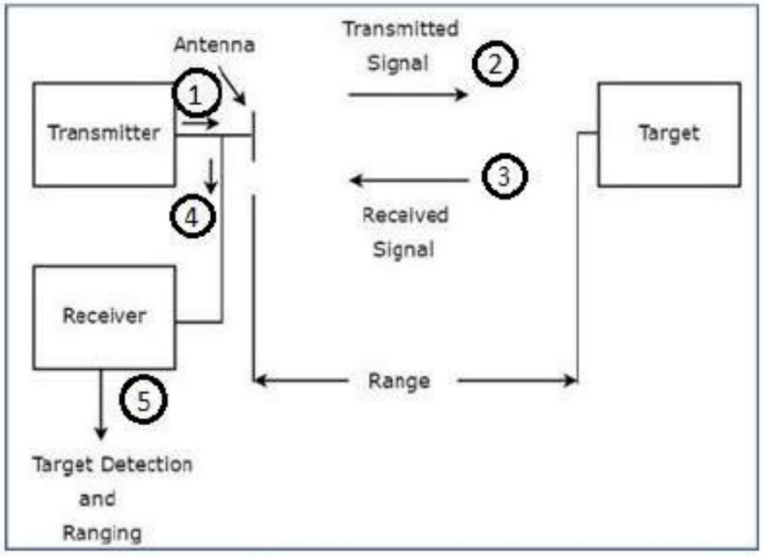
- Controlling the Air Traffic
- Ship safety
- Sensing the remote places
- Military applications

In any application of Radar, the basic principle remains the same.

Principle of RADAR (Radio Detection And Ranging): Radar is used for detecting the objects and finding their location. We can understand the **basic principle** of Radar from the following figure.

As shown in the figure, Radar mainly consists of a transmitter and a receiver. It uses the same Antenna for both transmitting and receiving the signals. The function of the **transmitter** is to transmit the Radar signal in the direction of the target present.

Target reflects this received signal in various directions. The signal, which is reflected back towards the Antenna gets received by the receiver.



Range: The distance between Radar and target is called **Range** of the target or simply range, R. We know that Radar transmits a signal to the target and accordingly the target sends an echo signal to the Radar with the speed of light, c.
Let the time taken for the signal to travel from Radar to target and back to Radar be 'T'. The two way distance between the Radar and target will be 2R, since the distance between the Radar and the target is R.
Now, the following is the formula for **Speed**.

$$\text{Speed} = \text{Distance} / \text{Time}$$

Hence, $\text{Distance} = \text{Speed} \times \text{Time}$

$$2R = C \times T$$

$$R = CT/2$$

Ques 12: Define modulation index for AM wave. (2 marks) (2022-23)

Sol.

Modulation Index μ or m_a: It states the depth or level of modulation that a carrier wave undergoes. In amplitude modulation, modulation index is defined as the ratio of amplitudes of modulating and carrier signals.
According to equation (3)

$$am(t) = (A_c + A_m \cos w_m t) \cos w_c t$$

Or, $$am(t) = A_c [1 + (A_m/A_c)\cos w_m t] \cos w_c t$$

According to the definition of modulation index,

$$\mu = m_a = A_m/A_c \quad \text{---------- (4)}$$

We will get the **percentage of modulation**, just by multiplying the modulation index value with 100.
Hence, $$am(t) = A_c [1 + m_a \cos w_m t] \cos w_c t \quad \text{---------- (5)}$$

Ques 13.

An audio frequency signal $10\sin 2\pi \times 500t$ is used to amplitude modulate a carrier of $50\sin 2\pi \times 10^3 t$. Calculate:

(i) Modulation index
(ii) Amplitude of Each side band
(iii) Total power delivered to the load of 2 KΩ.
(iv) Bandwidth

Sol.

(i) $\mu = \frac{A_m}{A_c} = \frac{10}{50} = 0.2$

(ii) Amplitude of each side band

$= \frac{m_a \cdot V_c}{2}$

$= \frac{0.2 \times 50}{2} = 5$

(iii) Total power delivered

$P_t = P_c \left(1 + \frac{m_a^2}{2}\right)$

$= \frac{V_c^2}{2R} \left(1 + \frac{0.2^2}{2}\right)$

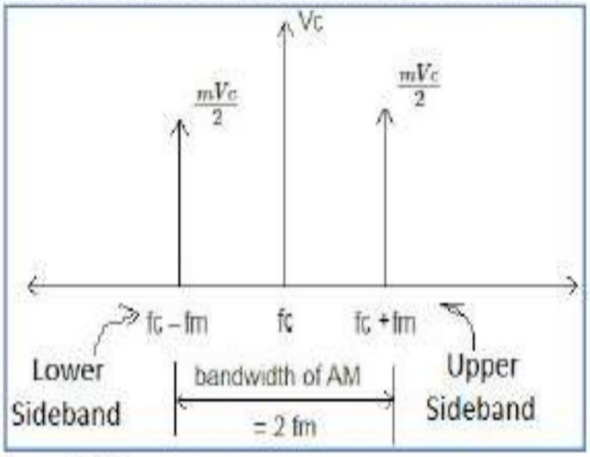
$= \frac{(50)^2}{2 \times 2 \times 10^3} (1.02)$

$= \frac{2500}{4000} (1.02)$

$= 0.625$ Watt

Ques 14. Derive the transmission efficiency and total power of amplitude modulated wave assuming message and carrier wave as sinusoidal wave.

Sol.



The amplitude of Upper Sideband = $m_a V_c/2$

The amplitude of Lower Sideband = $m_a V_c/2$

The amplitude of Central Band = V_c

As Power Content in a wave = V_{rms}^2/R

Hence, Carrier Power $P_c = (V_c/\sqrt{2})^2/R = V_c^2/2R$

Upper Sideband Power $P_{USB} = (m_a V_c / 2\sqrt{2})^2 / R = m_a^2 V_c^2 / 8R$

And, Lower Sideband Power $P_{LSB} = (m_a V_c / 2\sqrt{2})^2 / R = m_a^2 V_c^2 / 8R$

Hence, Total Sideband Power $P_{SB} = 2m_a^2 V_c^2 / 8R = m_a^2 V_c^2 / 4R$

Hence, total power content in AM wave

$P_t = P_c + P_{USB} + P_{LSB} = P_c + P_{SB}$

Here, $P_c = V_c^2 / 2R$ and $P_{SB} = m_a^2 V_c^2 / 4R = P_c m_a^2 / 2$

Or, $P_t = P_c + P_{SB}$

Or, $P_t = P_c + P_c m_a^2 / 2$

Or, $P_t = P_c (1 + m_a^2 / 2)$ Hence,

Fractional Sideband Power content in AM Wave (Transmission Efficiency)

$P_{SB} / P_t = [P_c m_a^2 / 2] / [P_c (1 + m_a^2 / 2)]$

$= (m_a^2 / 2) / (1 + m_a^2 / 2)$